HESSI IDPU Power Controller Specification
HSI_IDPU_008E
1999-Mar-17 D. W. Curtis

1. Introduction

This document is a specification for the IDPU power controller card. The Power Controller is a VME form factor card in the IDPU VME card rack. It contains a variety of power switches, controls, and monitors, plus some thermistor and other monitors. It is controlled and monitored via the IDPU backplane as called out in Reference 1. The card includes a single Actel A14100A FPGA, which contains all of the digital circuitry including the backplane interface, a tree of analog multiplexers connected to the backplane analog signal, a number of DACs providing control voltages, plus analog conditioning and power switch circuits. The board has 4 connectors:

- The IDPU Backplane Connector
- The IPC/CPC Interface Connector
- The Imager Interface Connector
- The Spectrometer Interface Connector

1.1 Related Documents

These documents are available on the web at:

ftp://apollo.ssl.berkeley.edu/pub/hessi/

[1] HESSI IDPU Backplane Signals (HSI_SYS_019)
[2] HESSI IDPU to Spacecraft ICD (HSI_SYS_001)
[3] HESSI IDPU VME Card Specification (HSI_IDPU_011)
[4] HESSI IDPU VME Chassis ICD (HSI_SYS_011)
[5] HESSI Instrument Harness Specification (HSI_SYS_022)

1.1. *Board Layout Issues*

The Power Controller card shall have a 6U-VME card form factor with a single P1 backplane connector as shown in reference 3. Three front pannel connectors interface with the IPC, CPC, Imager, RAS, and Spectrometer (IDPU-J2, IDPU-J3, and IDPU-J4). The location of these connectors is shown in reference 4.

The edges of the card are held in the chassis by wedgelocks indicated in reference 3. A spacer is required between the board and the wedgelock which can be extended onto the board in whatever form is required to act as a heat sync for any hot component (nominally any component dissipating more than 100mW).

The pinout of the backplane connector (P1) is called out in Reference 1. The pinout of the other connectors is called out in reference 5.

A shield board must be attached to the Power Controller card to provide RF shielding in the IDPU chassis and to provide added stiffness to the board. This shield board shall be made from 0.034" PCB material plated on one side, and attached to the solder side of the ADP via 0.100"-0.125" spacers and screws. At least one of these screws must connect the shield board plated side electrically to signal ground on the Power Control board. To provide adequate stiffness, there needs to be ate least 3 attachment points along the long edges of the board and 2 across the middle. Some of these screws can be the same ones used for connector mounting. The dimensions of the shield board shall be the same as the Power Control board (as indicated in reference 2), less 0.4" on each side to avoid the card guides.

2. IDPU Backplane Interface

The IDPU backplane is specified in Reference 1. The power controller register addressing range are as indicated in that document; the individual register addresses are called out in Table 2-1 and 2-2.

The interface to the backplane and all other digital electronics for the power Controller shall be contained in an Actel A14100A FPGA.

The backplane reset shall set all power switch control registers to the OFF.

Table 2-1 Register Addresses

Address (Hex)	Read / Write	Register Name	Contents
A0	W	DETHV12	Detector HVPS DAC settings, LSB = #1, MSB = #2 (see section 3.2.3)
A1	W	DETHV34	Detector HVPS DAC settings, LSB = #3, MSB = #4 (see section 3.2.3)
A2	W	DETHV56	Detector HVPS DAC settings, LSB = #5, MSB = #6 (see section 3.2.3)
A3	W	DETHV78	Detector HVPS DAC settings, LSB = #7, MSB = #8 (see section 3.2.3)
A4	W	DETHV9	Detector HVPS DAC settings, LSB = #9, MSB = Spare DAC #1 (see section 3.2.3)
A5	W	PDHV	Particle Detector HV DAC setting = LSB, MSB = Spare DAC #2 (see section 3.1.7)
A6	W	CPC_MAIN	Amplitude value for CPC Main 60Hz control signal = LSB. MSB = Unused (see section 3.3.1)
A7	W	CPC_BAL	Amplitude value for CPC Balancer 60Hz control signal = LSB. MSB = Unused (see section 3.3.1)
A8	R/W	CPC_PHASE	Phase value for CPC Balancer 60Hz control signal = LSB (0-255 = 0-350 degrees). MSB = Balancer

			Waveform Table number (0-7) (see section 3.3.1)
A9	R/W	ACTUATOR	Actuator Control, 4 LSB (Bite 0-3), encoded: 0 = All Off 1 = Shutter Lock-down 2 = Shutter #1 In 3 = Shutter #1 Out 4 = Shutter #2 In 5 = Shutter #2 Out 6 = Shutter #1 Unstick 7 = Shutter #2 Unstick 8 = RAS Shutter Primary 9 = RAS Shutter Backup A = Vacuum Valve Primary B = Vacuum Valve, Backup C-E = Spare F = Shutter Unstick Enable Bit 4: Actuator Supply Enable (1=enabled), to IPC. Bits 5-15: Unused (see section 3.1.4)
AA	R/W	IMAGER_HTR	Imager Heater Controls, unencoded , 1=On: Bit 0 (LSB): Upper Grid Tray Primary Bit 1: Upper Grid Tray Backup Bit 2: Lower Grid Tray Primary Bit 3: Lower Grid Tray Backup Bits 4-15: Unused (see section 3.1.3)
AB	R/W	CP_HTR	Cold Plate (Zener) Heater Enables, unencoded, 1=On: Bit 0-2: Enable zener 1-3 Bit 3: Source Supply (100V) Enable (1=enabled), to IPC Bit 4-15: Unused
AC	R/W	SWITCH	Miscellaneous Switches (1=On): Bit 0: High Voltage 28V Force On (see section 3.2.1) Bit 1: RAS Heater (see section 3.1.3) Bit 2: Spare 28V switch (see section 3.1.3) Bit 3: CPC Restart (see section 3.3.5) Bit 4: Shutter Pretension Sensor Power switch (see section 5.1.1) Bit 5: High Voltage 28V Force Off (see section 3.2.1) Bit 6-15: Spares (Bits 6-7 should come out of the FPGA)
AD	R	ACT_IMPED	Actuator Status (impedance readback): Bit 0 = Shutter Lock-down Bit 1 = Shutter #1 In

			Bit 2 = Shutter #1 Out Bit 3 = Shutter #2 In Bit 4 = Shutter #2 Out Bit 5 = Shutter #1 Unstick Bit 6 = Shutter #2 Unstick Bit 7 = RAS Shutter Primary Bit 8 = RAS Shutter Backup Bit 9 = Vacuum Valve Primary Bit 10 = Vacuum Valve, Backup Bit 11-15 = Unused (see section 3.1.4)
AE	R	ACT_SW	Actuator Status (switch readback): Bit 0 = Shutter Lock-down Bit 1 = Shutter #1 In Bit 2 = Shutter #1 Out Bit 3 = Shutter #2 In Bit 4 = Shutter #2 Out Bit 5 = Shutter #1 Pretension (see section 5.1.1) Bit 6 = Shutter #2 Pretension (see section 5.1.1) Bit 7 = Vacuum valve Bit 7-15 = Unused (see section 3.1.4)
AF	R	STATUS	Miscellaneous Status: Bit 0: High Voltage 28V Over-Current (1=tripped, 0=normal) (see section 3.2.1) Bit 1: CPC_Disable signal (see section 3.3.5) Bit 2: High Voltage 28V Status (1=on, 0=off) (see section 3.2.1) Bit 3-7 = Spare (Bits 3-7 should come out of the FPGA) Bits 8-15: CPC Main Phase (current value of the 8-bit counter that addresses the CPC Main waveform; cycles 0-255 at about 60Hz)
F0	W	AHKP_SELECT	See Reference 1 and Table 2.1-1

2.1. *Analog Housekeeping*

The IDPU backplane has a single analog signal that is shared by all the VME cards and measured by an ADC on the Data Controller card. The Power Controller shall have a tree of analog H508A multiplexers driving that line. Eight multiplexers shall each drive an input of a nineth multiplexer via unity gain op-amps. The output of the nineth multiplexer shall be connected to the analog signal on the backplane. The 8 input multiplexers shall all be wired to 3 address lines provided by the FPGA, and their enable lines shall be wired active. The eighth multiplexer shall be wired to 3 more address lines from the FPGA, and its enable shall also be provided by the FPGA. The address is

provided by the backplane as specified in reference 1, and the enable shall only be active when the address is in the Power Controller's address range (C0-FF hex). Unused multiplexer inputs can be tied to SGND (signal ground).

All inputs to the tree shall not exceed +/- 2.5V , and shall have a source impedance of <50kohms.

Table 2.1-1 Power Controller Analog Housekeeping Measurements

AHKP_ Select	Signal	Measurement
C0	VP5D	+5D Voltage Monitor (see section 3.1.1)
C1	VP5DR	+5D Regulated Voltage Monitor (see section 3.1.1.1)
C2	VP5	+5 Voltage Monitor (see section 3.1.1)
C3	VM5	-5 Voltage Monitor (see section 3.1.1)
C4	VP12	+12 Voltage Monitor (see section 3.1.1)
C5	VM12	-12 Voltage Monitor (see section 3.1.1)
C6	VP15	+15 Voltage Monitor (see section 3.1.1)
C7	VP28	+28 Voltage Monitor (see section 3.1.1)
C8	VP100	+100 Voltage Monitor (see section 3.1.1)
C9	VACT	Actuator Voltage Monitor (see section 3.1.4)
CA	VP28SW	+28 Switched Voltage Monitor (see section 3.1.3)
CB	VP28HV	+28 HV Supply Monitor (see section 3.2.1)
CC	VINSHTR	Instrument Heater Voltage Monitor (see section 3.1.5)
CD	Spare	
CE	Spare	
CF	Spare	Allocated to SAS X input to the IDPU simulator
D0	VHVMON1	HV supply #1 Voltage Monitor (see section 3.2.4)
D1	VHVMON2	HV supply #2 Voltage Monitor (see section 3.2.4)
D2	VHVMON3	HV supply #3 Voltage Monitor (see section 3.2.4)
D3	VHVMON4	HV supply #4 Voltage Monitor (see section 3.2.4)
D4	VHVMON5	HV supply #5 Voltage Monitor (see section 3.2.4)
D5	VHVMON6	HV supply #6 Voltage Monitor (see section 3.2.4)
D6	VHVMON7	HV supply #7 Voltage Monitor (see section 3.2.4)
D7	VHVMON8	HV supply #8 Voltage Monitor (see section 3.2.4)
D8	VHVMON9	HV supply #9 Voltage Monitor (see section 3.2.4)
D9	VUGTHTRP	Primary Upper Grid Tray Heater Voltage Monitor (3.1.3)
DA	VUGTHTRB	Backup Upper Grid Tray Heater Voltage Monitor (3.1.3)
DB	VLGTHTRP	Primary Lower Grid Tray Heater Voltage Monitor (3.1.3)
DC	VLGTHTRB	Backup Lower Grid Tray Heater Voltage Monitor (3.1.3)
DD	VRASHTR	RAS Heater Voltage Monitor (3.1.3)
DE	VSPAREHTR	Spare 28V switch Voltage Monitor (3.1.3)
DF	Spare	Allocated to SAS Y input to the IDPU simulator

E0	TUGT1	Upper Grid Tray Temperature Monitor #1 (see section 4.3)
E2	TUGT2	Upper Grid Tray Temperature Monitor #2 (see section 4.3)
E2	TUGT3	Upper Grid Tray Temperature Monitor #3 (see section 4.3)
E3	TUGT4	Upper Grid Tray Temperature Monitor #4 (see section 4.3)
E4	TLGT1	Lower Grid Tray Temperature Monitor #1 (see section 4.3)
E5	TLGT2	Lower Grid Tray Temperature Monitor #2 (see section 4.3)
E6	TLGT3	Lower Grid Tray Temperature Monitor #3 (see section 4.3)
E7	TLGT4	Lower Grid Tray Temperature Monitor #4 (see section 4.3)
E8	TRAS1	RAS Temperature Monitor #1 (see section 4.3)
E9	TRAS2	RAS Temperature Monitor #2 (see section 4.3)
EA	TIPC	IPC Temperature Monitor (see section 3.1.9)
EB	TCPC	CPC Temperature Monitor (see section 3.3.3)
EC	TIDPU	IDPU Temperature Monitor (see section 2.2.1)
ED	PDTMON	Particle Detector Temperature Monitor (see section 2.3)
EE	TSHUT	Shutter Actuator Temperature Monitor (see section 5.4)
EF	TRAD1	Cryocooler / Radiator Temperature Monitor (see section 5.4)
F0	TRAD2	Cryocooler / Radiator Temperature Monitor (see section 5.4)
F1	Spare	
F2	Spare	
F3	TCP1	Cold Plate Temperature Monitor #1 (see section 5.5)
F4	TCP2	Cold Plate Temperature Monitor #2 (see section 5.5)
F5	TCT1	Cold Tip Temperature Monitor #1 (see section 5.5)
F6	TCT2	Cold Tip Temperature Monitor #2 (see section 5.5)
F7	TTS	Thermal Shield Temperature Monitor (see section 5.5)
F8	IMON5D	+5D Current Monitor from the IPC (see section 3.1.2)
F9	IMON5	+/-5 Current Monitor from the IPC (see section 3.1.2)
FA	IMON12	+/-12 Current Monitor from the IPC (see section 3.1.2)
FB	IMON15	+15 Current Monitor from the IPC (see section 3.1.2)
FC	IMON28	+28 Current Monitor (see section 3.2.1)
FD	CPCMain	CPC Main Waveform (see section 3.3.1)
FE	CPCBal	CPC Balancer Waveform (see section 3.3.1)
FF	ACCEL	Accelerometer (See section 5.6)

2.2. *Thermistor Conditioning*

There shall be a number of YSI 10Kohm Thermistors in the Spectrometer, Imager, and IDPU/IPC/CPC that shall be conditioned by the Power Controller and routed to the Multiplexer tree described in section 2.1. The thermistors shall be conditioned simply by attaching the return leg to SGND and pulling the other leg up to a +2.5V reference voltage via 30Kohms. A 0.1uF (TBR) bypass capacitor to reduce noise shall be included across the thermistor. The thermistor shall then be connected directly to the analog multiplexer input.

2.2.1. IDPU Thermistor

The IDPUTMON thermistor shall be on the Power Controller board, attached to the side rail away from any of the power dissipators.

2.2.2. Particle Detector Thermistor

The Particle Detector has a thermistor that is connected to the Power Controller via the backplane. No thermistor return is provided for this thermistor – it is attached to SGND inside the Particle Detector. Otherwise this thermistor is treated like the others.

3. IPC/CPC Interface (IDPU-J2)

Connector IDPU-J2 carries all interface signals from the IDPU to the Instrument Power Converter (IPC), which includes the instrument High Voltage and Low Voltage power converters, and the Cryo Power Converter (CPC).

3.1. *IPC Low Voltage Supply Interface*

3.1.1. Low Voltage Supplies

The IPC provides a number of regulated low voltages to the IDPU VME chassis via the Power Controller card, as shown in Table 3.1-1. Nominal current levels are shown.

Table 3.1-1 Low Voltage Supply Characteristics

Supply	Characteristics
+5D	5.4V -0/-10% 1A (digital)
DGND	+5D Return
+5	5.4V -0/+10% 1A (analog)
-5	-5.4V +0/-10% 1A (analog)
+12	+12.5V –0/+10% 1A (analog)
-12	-12.5V +0/-10% 1A (analog)
+15	+15.0V –0/+10% 0.1A (analog)
SGND	Return for +/-5, +/-12, +15
+28	+28V +/-5%, 45mA
+28 Ret	Return for +28V
+100V	100V +/-5% 150mA

All of these supply voltages shall be appropriately divided and monitored via the analog housekeeping tree described in section 2.1. The dividers shall provide a 50kohm source impedance to the multiplexer input.

- +5D and DGND is routed to the backplane and also to a Low Dropout regulator described in section 3.1.1.1. DGND is used by the FPGA.
- +5, -5, +12, -12, and +15 may be used to power analog circuits on the Power Controller, and are also connected to the backplane. +/-12 is provided to the HV

power supplies (see section 3.2.2). +5 and -12 are routed to the Service Filter (see section 5.5).

- SGND is used as analog ground on the Power Controller and is also connected to the backplane. It is also provided to the HVPS (section 3.2.2), CPC (section 3.3.1), and the Cryostat Temperature Sensor Conditioning Circuit (section 5.5).
- +28 / +28 Ret is switched and current monitor/limited by the Power Controller before being passed back to the IPC to power the HVPS (see section 3.2.1).
- The +100V supply is used to power the Spectrometer cold plate heaters (see section 5.3). The routing of the 100V supply must be kept separated from other signals per NHB5300.4(3K).
- SGND DGND, and 28V Ret shall be kept separate.

3.1.1.1 +5D Low Dropout (LDO) Regulator

The Power Controller shall include a Low Dropout Regulator to convert the 5.4V "+5D" digital supply from the IPC into a 5.0V digital supply. The converter shall be capable of handling up to 1 Amp, and shall produce 5.0V +/-5%, starting with 5.4V -0/+10%. The local digital circuits (the FPGA), as well as the backplane, shall be connected to the output of this regulator.

3.1.2. IPC Current Monitors

The IPC low voltage supply provides current monitor signals to be connected to the analog multiplexers without further conditioning: IMON5D, IMON5, IMON12, and IMON15 as shown in table 2.1-1.

3.1.3. Switched Power

The Spacecraft “Switched Power” service is routed to the IPC, and from there to the Power Controller board via IDPU-J2. This 28V service and its return are used to power four heaters via FET switches on the Power Controller. The FET switches are individually controlled by the FPGA via IDPU backplane command. The FET switches must have <0.1ohm impedance. The heaters are listed in Table 3.1.3-1.

Table 3.1.3-1 28V Heater Services

Service	Description	Heater Power
UGTHTRP	Imager Upper Grid Tray Heater Primary	15W
UGTHTRB	Imager Upper Grid Tray Heater Backup	15W
LGTHTRP	Imager Lower Grid Tray Heater Primary	15W
LGTHTRB	Imager Lower Grid Tray Heater Backup	15W
RASHTR	RAS Heater	5W (TBR)
SPAREHTR	Spare switch	TBD

The switched power supply and the outputs of the switches shall be appropriately divided and monitored via the analog housekeeping tree described in section 2.1

3.1.4. Actuator Power

The IPC includes a special power converter off the Switched Power source to run the actuators. A logic signal from the Power Controller board to the IPC (via a latch in the FPGA set via the backplane) turns on the actuator power supply. An enable plug on the IPC must be also be installed in order for the actuator power to be turned on. This supply generates about 10V at up to 5A. The actuator supply has a separate return line that should be kept separate from other returns.

The actuator supply is routed to eleven low impedance FET switches (<0.05 ohms). The FETs shall be capable of handling 5A for 4 seconds (plus design margin). Some of the actuator circuits include current limiting resistors (see Table 3.1.4-1). Some actuators shall provide a status signal that is connected to ground in one position and open in the other (marked 'Signal' in the Status Measurement column of Table 3.1.4-1). These status lines shall be pulled to +5V Digital (Regulated) via 10Kohms and routed to a status register in the FPGA. All actuators also have a status measurement based on measuring the impedance on the actuator line (the actuators have an automatic cut-off when the reach their desired location which will cause the impedance to go high). This is accomplished by pulling up the actuator line to +5V digital (Regulated) via 100Kohms. The actuator line is connected to a status register in the FPGA via a 10Kohm series resistor with a clamp diode to +5 Digital (to protect the FPGA).

Only one actuator shall be powered at a time. This rule is enforced by the FPGA, by encoding the desired actuator in the command register, and using a one-of-N decoder to drive the actuator power switch.

The Shutter Unstick actuators are 1-time devices that disable further use of the shutters. To minimize the risk of accidental firing of these actuators, the system shall require an enable signal be sent first. This involves pulsing the Shutter Unstick Enable signal prior to firing the actuator. The Unstick Enable shall be automatically disabled on reset and at each 1-second tick.

Table 3.1.4-1 Actuator Characteristics

Actuator	Type	Current Limit Series Resistor	Status Measurement	Destination
RAS Shutter Prime	One-time	3 ohm 1W RWR81 (***)	-	IDPU-J3
RAS Shutter Backup	One-time	3 ohm 1W RWR81 (***)	-	IDPU-J3
Vacuum Valve Prime	One-time	No	Signal	IDPU-J4
Vacuum Valve Backup	One-time	No	Signal (**)	IDPU-J4
Shutter Lock-down	One-time	No	Signal	IDPU-J4
Shutter #1 Unstick	Emergency	No	Signal (*)	IDPU-J4
Shutter #2 Unstick	Emergency	No	Signal (*)	IDPU-J4
Shutter #1 In	Multiple	No	Signal	IDPU-J4

Shutter #1 Out	Multiple	No	Signal	IDPU-J4
Shutter #2 In	Multiple	No	Signal	IDPU-J4
Shutter #2 Out	Multiple	No	Signal	IDPU-J4

(*) – Uses the same status signal as Shutter In/Out
(**) – This is a redundant actuator. It uses the same status signal as the prime.
(***) - Prime and backup RAS shutter actuators can share the series resistor (put it upstream of the switches).

3.1.5. Instrument Heater

The Instrument Heater service is provided by the spacecraft to the IPC, and from the IPC to the IDPU via IDPU-J2 on the Power Controller Board. This 28-volt service and its return shall be routed to the backplane, from which it is wired to the IDPU thermostat and heater. It shall also be routed by the Power Controller to the Spectrometer via IDPU-J4 (see section 5.2) and the CPC via IDPU-J2 (see section 3.3.2). The Instrument Heater return shall be kept separate from the other returns.

The Instrument Heater supply shall be appropriately divided and monitored via the analog housekeeping tree described in section 2.1. The divider shall provide a 50kohm source impedance to the multiplexer input.

3.1.6. 100V Cold Plate Heater Supply Enable

The Power Controller shall supply a logic signal to the IPC to enable the 100V Cold plate Heater supply. This is a logic level signal provided by the FPGA.

3.1.7. Particle Detector Bias Supply Control

The Power Controller shall provide a control signal to the IPC for the Particle Detector Bias Supply. This signal shall be set by an 8-bit DAC in the range 0-5V, set by the FPGA.

3.1.8. Synchronization Signal

The Power Controller shall provide a 128KHz (TBR) clock signal to the IPC to synchronize the power converter. This clock shall be provided by the FPGA by dividing down the 2^{20}Hz timing clock.

3.1.9. IPC Thermistor

The IPC shall include a Thermistor to be conditioned and routed to the analog housekeeping tree as indicated in section 2.1.

3.2. *IPC High Voltage Supply Interface*

3.2.1. 28V Supply

The Power Controller passes the 28V supply from the IPC through a FET switch, current limiter, and current monitor circuit prior to returning it to the IPC HV Supply where it provides the primary power for the HV supplies. The current monitor (IMON28) and

output voltage level (VP28HV) shall be routed to the analog housekeeping MUX tree described in section 2.1. The current limiter shall be set to 0.2A (TBR), and shall act as a circuit-breaker (the switch turns off in the event of over-current trip). The circuit-breaker shall be reset (turning the HV 28V on) by a pulse from the FPGA (High Voltage 28V Force On), and over-ridden by a constant active level on the same signal (this is required to avoid tripping the circuit-breaker during the inrush transient for a TBD interval). A second signal forces the 28V off (trips the circuit breaker) (High Voltage 28V Force Off). Two sense signals are provided: Over current detection (High Voltage 28V Over-Current), and the status of the circuit breaker (High Voltage 28V Status. +28V return is also provided directly from the IPC.

3.2.2. +/-12V Supply

The power controller shall route the +12V and –12V supply and SGND from the IPC (see section 3.1.1) back to the IPC HV supplies.

3.2.3. HV Control Levels

The nine detector HV supplies shall be individually programmed by a 0-5V levels provided by DACs on the Power Controller. These DACS shall be controlled by registers in the FPGA set by backplane command. There are also 2 spare DACs whose outputs are currently not used.

3.2.4. HV Voltage Monitors

Output voltage monitors shall be provided by each of the nine HV supplies. The voltage on the monitor is 0-5V (TBR). These shall be routed to the analog multiplexer tree described in Section 2.1.

3.3. *CPC Interface*

3.3.1. CPC Controls

The Power Controller shall provide two control signals to the CPC to set the waveforms for the Cryocooler and Balancer. These signals shall be 58.6Hz (+0/-0.1Hz) waveforms with programmable amplitude (0-5V maximum with a 2.5V offset) and programmable relative phase. The two amplitudes and the relative phase information shall be provided by the backplane to the FPGA. The FPGA shall generate the wavforms using a PROM look-up table and DACs. The waveforms shall include 256 points/cycle and 1% amplitude resolution, and shall be filtered to remove digitization noise. The Amplitudes shall be programmable from 5 to 100% of full scale without losing the 1% amplitude resolution. The relative phase shall be programmable to a resolution of at least 1.4 degree. SGND shall be provided as a reference level for these signals and the synchronization signal (see section 3.3.4).

The PROM look-up table shall include 8 waveforms. The Main Cryocooler waveform shall always use Table number 0 (a sine wave). The Balancer waveform shall use one of the 8 tables (number 0-7), as selected by a programmable register in the FPGA.

The outputs shall have a passive low-pass filters to minimize transients during power-up and power-down of the instrument power. The Main service filter bandwidth shall be only slightly greater than 60Hz (enough higher to ensure <1% phase lag). The Balancer service filter shall have 250Hz bandwidth.

The waveforms (after the filtering) shall be provided to the analog housekeeping multiplexer as indicated in section 2.1.

3.3.2. CPC Heater

The Instrument Heater 28V supply (see section 3.1.3) and Return shall be routed through the Power Controller to the CPC.

3.3.3. CPC Thermistor

The CPC shall include a Thermistor to be conditioned and routed to the analog housekeeping tree as indicated in section 2.1.

3.3.4. CPC Synchronization Signal

The Power Controller shall provide a 128KHz (TBR) clock signal to the CPC to synchronize the power converter. This clock shall be provided by the FPGA by dividing down the 2^{20}Hz timing clock.

3.3.5. CPC Disable and Restart

The CPC has an overcurrent trip circuit. The state of this trip is provided to the Power Controller over IDPU-J2 as the digital signal CPC_Disabled. This signal must be pulled up to +5.0V digital via 10Kohms and routed to the FPGA.

The CPC overcurrent trip can be reset by the CPC_Restart signal from the Power Controller via IDPU-J2. This signal powers the diode of an optocoupler, and should be capable of 10mA at 1V-2V. Since an FPGA output pin cannot drive 10mA directly, a FET or transistor switch must be used, powered by +5.0V digital, and followed by a current limiting series resistor of 300 ohms (TBR).

4. Imager Interface (IDPU-J3)

IDPU-J3 carries power and thermistor services to the Imager and RAS from the Power Controller.

4.1. *RAS Actuator*

The RAS primary and backup actuator services described in 3.1.4, together with the Actuator supply return, shall be routed to RAS via IDPU-J3. The RAS shutter position shall be measured via the actuator service impedance as described in section 3.1.4.

4.2. *Grid Tray Heaters*

There are primary and backup heaters on the Lower Grid Tray (LGT) and Upper Grid Tray (UGT). The Power Controller provides switched 28V and Switched Power return to these heaters via IDPU-J3 as described in Section 3.1.3.

4.3. *Thermistors*

The Imager contains 10 thermistors, to be conditioned as described in section 2.2. Both leads of each thermistor are separately wired to IDPU-J3. We hope to get 0.1 degree resolution (one part in 2000 in signal) on these thermistors, so noise should be minimized.

- 4 Upper Grid Tray Thermistors
- 4 Lower Grid Tray Thermistors
- 2 RAS Thermistors

4.4. *RAS Temperature Sensor*

There is a spacecraft-conditioned temperature sensor in the RAS that is routed through the Power Controller to the IDPU Backplane. The power controller passes the temperature sensor signal and return to the backplane with no conditioning.

4.5. *RAS Heater*

RAS includes a heater. The Power Controller provides switched 28V and Switched Power return to these heaters via IDPU-J3 as described in Section 3.1.3.

5. Spectrometer Interface (IDPU-J4)

IDPU-J4 carries power and temperature monitoring signals to the Spectrometer from the Power Controller.

5.1. *Actuators*

The Power Controller controls 9 actuators in the Spectrometer. Each service includes switched power, actuator return, and, in some cases, a position status signal, as described in section 3.1.4.

- Vacuum Valve, (2 Services)
- Shutter Lock-down
- Shutter Unstick #1 & #2 (2 services)
- Shutter In and Out, #1 and #2 (4 services)

5.1.1. Shutter Pretension Sensor

The In/Out actuators also have a pretension sensor, which is used to determine when it is safe to activate the opposing actuator. This sensor consists of a photodiode and phototransistor, interrupted by the pretensioning device. There are 2 sensors, one for each actuator; they are common for the In and Out state. The power controller must provide power to the photodiodes and sense the phototransistors.

Power is provided over a single common pin on the IDPU-J4 connector (ShutSensePower). The power shall be 5.4V taken from the +5D supply and switched with a FET or transistor controlled by the FPGA. The supply needs to provide about 200mA (limited by series resistors in the Shutter assembly). This power is returned in ShutSenseSGND, which should be tied to Digital Ground.

The two sense signals also appear on IDPU-J4 (Shut1ActState and Shut2ActState). These are conditioned by 10K pull-ups to +5.0V digital and routed to FPGA inputs.

5.2. *Cryocooler / Radiator Heater*

There is a thermostatically controlled heater on the Spectrometer Radiator to heat the Cryocooler to its operational temperature. The Power Controller routes Instrument Heater 28V and return to this heater as described in Section 3.1.3.

5.3. *Cold Plate Heaters*

The Cold Plate Heaters are three 70V Zener diodes inside the Spectrometer. The Power Controller includes individual switched current sources for each of these heaters based on the 100V supply described in section 3.1.1. The current sources shall be set to 70mA each (TBR).

5.4. *Thermistors*

The Spectrometer includes three thermistors that are conditioned and monitored as described in section 2.2. Both leads of each thermistor are separately wired to IDPU-J4.

- Shutter Actuator Thermistor
- Two Cryocooler / Radiator Thermistors

5.5. *Cryostat Temperature Sensors*

The Cryostat contains 5 temperature sensors that are conditioned in the “Service Filter” box on the side of the cryostat. The conditioned values (0 to 2.5V TBR) are passed to the Power Controller via IDPU-J4. The power controller passes these signals to the analog multiplexer tree described in section 2.1. without further conditioning other than an R-C noise filter (1K, 0.1uF TBR).

- Cold Tip Temperature Monitor #1
- Cold Tip Temperature Monitor #2
- Cold Plate Temperature Monitor #1
- Cold Plate Temperature Monitor #2
- Thermal Shield Temperature Monitor

The temperature sensor conditioning circuit in the Service Filter requires +5 and -12 (analog) and SGND, which is provided by the Power Controller via IDPU-J4.

5.6. *Accelerometer*

The cryostat has an accelerometer to measure vibrations caused by the cryocooler. This accelerometer is contained in the "Service Filter", and is powered by the +5 analog supply (see section 5.5). The accelerometer generates a 0-5V low impedance output, which must be conditioned prior to being input into the analog housekeeping tree described in section 2.1. Conditioning shall consist of a resistor divider to reduce the

voltage range to 0-2.5V, plus a capacitor on the output of the divider to provide a low-pass filter at 300Hz.