Data Controller Board Programming Summary

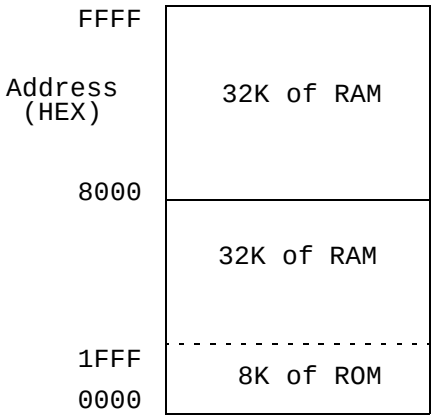
Memory and I/O Decode
Revision B
16 July 1999

HSI_IDPU_012D

1.0 Data Controller Memory Mapping

The BCF decodes and latches the 8085 address as follows:

For memory accesses (when the 8085 signal IOM=0), the ROM and RAM are mapped concurrently to address zero. It results in the following memory map:



The ROM appears only once (does not “wrap”) within the 32K memory space allotment. The RAM aliases 2X within the 64K processor memory space. When the ROM is powered on (default at reset) all reads between addresses 0-1FFF Hex access ROM, but all writes access RAM. (With the ROM powered on, the RAM can still be read at address 8000 Hex.) When the ROM is powered off (controlled by a register bit) all reads and writes access RAM only.

2.0 Data Controller I/O Memory Mapping

The IO space (when the 8085 signal IOM=1) is divided between Data Controller subsystems and the IDPU backplane. It is apportioned as follows:

IO Address (Hex)	Selected Subsystems
0-8	Detector Interface Cards
9	Aspect Data Processor
A	Power Controller
B	Bus Controller FPGA (internal registers)
C	Packet Formatter FPGA (internal registers)
D	DMA Controller (82C37)
E	PFF MemoryTest Mode
F	IDPU backplane Broadcast Mode

TABLE 1. IDPU Memory Map

For programming details, see specifications relating to selected subsystems. The Data Controller registers are outlined below:

Address	Read Register	Write Register
B0	Particle Detector Counter - A 8 bit compressed count, latched 8 times/ second.	Power Switches Bit 0: ROM Off setting this bit to zero turns off power to the ROM. It defaults to one at reset
B1	Particle Detector Counter - B 8 bit compressed count, latched 8 times/ second.	Enables/Controls Bit 0: Enable Fast Rate Counters Bit 1: Enable Monitor Rate Counters Bit 2: Uplink Enable - Arms the enable for the command DMA channel. Bit 3: Disable Overcurrent Shutdown - Disables the ADCSHUTDOWN signal. Bits 0 and 1 (when set to one) enable the Fast Rate or Monitor Rate counter packet collection. All Enables default to zero at reset.
B2	Bus Extension Register This register holds the upper 8 bits of data from the last IDPU bus read.	Bus Extension Register This register drives the upper 8 bits of the next IDPU bus write.
B3	Not used	Any write to address B3 touches the watchdog timer.

Address	Read Register	Write Register
B4	ADC Data, lower byte NOTE: the Analog channel must be selected (and IDPU bus broadcast), and an SOC pulse must be issued (at address B5).	ADC Control Bit 0: ADC Shutdown - defaults to zero at reset. (When ADC Shutdown=0, the ADC is in "nap mode"; otherwise, the ADC is ready to convert.)
B5	ADC Data, upper byte	Any write to address B5 pulses the SOC line of the ADC, causing a conversion. Data can subsequently be read back at addresses B4 and B5.
B6	undefined	DAC Writes byte to Particle Detector Control DAC.
B7	undefined	Diagnostic Register Bits 7:0 of the CPU data bus are strobed into two separate latches, one is external, serving as a debug data bus, and the other is internal to the BCF. The internal diagnostic register is telemetered along with the Monitor Rate Data.
B8	BCF Status Register Bit 0: Uplink Parity Error Bit 1: ADC Overcurrent Detect (Latched) Bit 2: ADC Overcurrent Signal (Input to BCF, unlatched version direct from analog circuitry.) Bit 3: ADC overcurrent shutdown disable (bit 3 of Enables/Control register) Bit 4: Fast Rate Counters Enable (bit 0 of Enables/Control register) Bit 5: Monitor Rate Counters Enable (bit 1 of Enables/Control register) Bit 6 : Uplink Enable - follows bit 2 of Enables/Control register. Bit 7: ROMON - Bit 0 of Power Switch Register The Status register is telemetered along with the Monitor Rate Data.	BCF Pulse Register Bit 0: Clear Uplink Parity Error Bit 1: Clear ADC Shutdown Detect
B9	undefined	Transfer Request Mask Register Low A mask register which defaults to low at reset (all subsystems enabled). Setting any bit in this register disables transfer requests from the corresponding subsystem. Bits 7-0: Correspond directly to ETR[7:0]

Address	Read Register	Write Register
BA	undefined	Transfer Request Mask Register High A mask register which defaults to low at reset (all subsystems enabled). Setting any bit in this register disables transfer requests from the corresponding subsystem. Bit 0: ETR8 Bit 1: ADP Transfer Request
BB-BF	undefined	not used
C0	PFF Control Readback Directly reads back PFF Control Register	Control Register Bit 0: PF Memory Test mode setting this bit to one allows the processor to read and write the 32K x 16 Packet Formatter Memory. Bit 1: PF Memory Bank Select sets the upper bit (ADR14) of the PFF memory address. Bit 2: Telemetry Inhibit setting this bit halts the telemetry readout and causes a general reset of the packet readout subsystem (packet writing continues until memory fills). Bit 3: unused Bit 6-4: Internal Timer Interrupt Select Field Value -> Timer Frequency 0 - 8 Hz 1 - 16 Hz 2 - 32 Hz 3 - 64 Hz 4 - 128 Hz 5 - 256 Hz 6 - 512 Hz 7 - 1024 Hz Bit 7: Internal Timer Mode setting this bit causes the PFF to use internally generated clocks rather than the S/C inputs (1MHz and 1Hz). All Control Register bits are cleared to zero by reset.

Address	Read Register	Write Register
C1	PFF Status Readback Bit 0: Timer Interrupt (latched) Bit 1: One Second Interrupt (latched) Bit 2: DMA - EOP Interrupt (latched) Bit 5-3: Spares Bit 6: S/C Telemetry Inhibit (input RRECRDYF from the high speed telemetry I/F) Bit 7: SAFE - S/C status input	PFF Pulses Bit 0: Clear Timer Interrupt Bit 1: Clear One Second Interrupt Bit 2: Clear DMA-EOP Interrupt Bit 7: Clear Error Flags clears all Packet Collection related Error Flags, which are readable at address C2
C2	Packet Collection Error Status Readback Bit 0: Event Memory Full Error Bit 1: Event Long Packet Error Bit 2: Fast Rate Memory Full Error Bit 3: Fast Rate Long Packet Error Bit 4: Monitor Rate Memory Full Error Bit 5: Monitor Rate Long Packet Error Bit 6: ADP Short Packet Error Bit 7: ADP Long Packet Error	Not used
C3	Spare	Not used
C4	Seconds Register Low word: Bits[7:0]	Seconds Register Low word: Bits[7:0]
C5	Seconds Register Low word: Bits[15:8]	Seconds Register Low word: Bits[15:8]
C6	Seconds Register High word: Bits[7:0]	Seconds Register High word: Bits[7:0]
C7	Seconds Register High word: Bits[15:8]	Seconds Register High word: Bits[15:8]
C8	Instrument Header Register 1	Instrument Header Register 1: Bits[7:0] first byte shifted out as telemetry header
C9	Instrument Header Register 2	Instrument Header Register 2: Bits[7:0] 2nd byte shifted out as telemetry header
CA	Instrument Header Register 3	Instrument Header Register 3: Bits[7:0] 3rd byte shifted out as telemetry header
CB	Instrument Header Register 4	Instrument Header Register 4: Bits[7:0] 4th byte shifted out as telemetry header
CC	Instrument Header Register 5	Instrument Header Register 5: Bits[7:0] 5th byte shifted out as telemetry header
CD	Instrument Header Register 6	Instrument Header Register 6: Bits[7:0] 6th byte shifted out as telemetry header
CE	Subseconds Counter Bits[11:4]	not used
CF	Subseconds Counter Bits[19:12]	not used
E8	E8 through EB read back the PFF low data byte pointed to by the PFF Address Register. During this read cycle the upper data byte is latched into a register which can be read back at addresses EC-EF (see below).	Test Mode Data Register Low Byte
E9		Test Mode Data Register High Byte
EA		Test Mode Lower Address Register (maps to PFF Memory Address 7:0
EB		Test Mode Upper Address Register (data bits 5:0 map to PFF Memory Address 13:8) The PFF control register drives address bit 14.

Address	Read Register	Write Register
EC	Upper data byte of PFF memory, previously latched by read of E8-EC (see above).	spare
ED		Create Write strobe to PFF memory. Data in Test Mode data registers is written into the PFF memory address pointed to by the PFF Test Mode address registers.
EE		not used
EF		

TABLE 2. Data Controller I/O Register Memory Map

3.0 DIF Register Map

NOTE: X => Detector ID

Address	Read Register	Write Register
X0	Event Data - first 16 bits of a 32-bit event word	General Register/Controls Bit 0: Spare Register Output Bit 1: AFE Bit 2: TP (Test Pulser Power) Bit 3: Enable Overcurrent Shutdown Outputs are active high, with reset default to deasserted (low).
X1	Event Data - second 16 bits of a 32-bit event word	Global Enables/Controls Bit 0: EventRequest Enb Bit 1: Pulser Enb Bits 3-2: Test Mode Control Field 00 => Normal (test mode disabled) 01=> 1 MHz Clock = Event Strobe 10=> 62.5 KHz Clock = Event Strobe 11=> Pulser Output = Event Strobe Bits 7-4: Test Mode Parameter Field sets test mode upper energy bits
X2	Fast Rate - first of formatted fast rate data words, latched every “collect-time” clock. (dependent on CARD-ID)	Front Detector Enables Bit 0: Event Enb Bit 1: CSA Reset Enb Bit 2: Over Threshold Enb Bit 3: Decimation Enb Bit 4: Decimate Any Bit 5: Dither Enb
X3	Fast Rate - second of formatted fast rate data words, latched every “collect-time” clock. NOTE: CARD-IDs 0,1 and 2 supply only 16-bits of fast rate counter data, available at address X2 only.	Front Decimation Parameters Bit 3-0: Decimation Count Bit 7-4: Decimation Energy

Address	Read Register	Write Register
X4	BITS: 15-8: Front PreAmp Reset Count - a 16 bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Front Slow Channel Valid Count - a 17-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	Rear Detector Enables Bit 0: Event Enb Bit 1: CSA Reset Enb Bit 2: Over Threshold Enb Bit 3: Decimation Enb Bit 4: Decimate Any Bit 5: Dither Enb
X5	BITS: 15-8: Front Slow Channel Over ULD Count - a 9-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Front Fast Channel Valid Events - a 19-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	Rear Decimation Parameters Bit 3-0: Decimation Count Bit 7-4: Decimation Energy
X6	BITS: 15-8: Front Live Time Count - the 8 MSBs of the 20-bit “live-time” counter. Latched once/second BITS: 7-0: Rear Preamp Reset Count - an 18-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	
X7	BITS: 15-8: Rear Slow Channel Valid Count - a 14-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Rear Slow Channel Over ULD Count - a 8-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	Pulse Register Bit 0: Clear Latched Shutdown (Pulse)
X8	BITS: 15-8: Rear Fast Channel Valid Events - a 19-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Rear Live Time Count - the 8 MSBs of the 20-bit “live-time” counter	Pulser Frequency Select Bit 3-0: Select from 11 frequencies ranging from 1 Hz to 1KHz
X9-XB	Not used	Not used

Address	Read Register	Write Register
XC	DIF Status Bit 0: AFE Power Bit 1: Enable Overcurrent Shutdown Bit 2: Overcurrent Status - Latched overcurrent indicator, set by either of two inputs from the AFE, cleared by pulsing "Clear Latched Shutdown" (see Address X7). Bit 3: AFESHUTDOWN status line 0 Bit 4: AFESHUTDOWN status line 1 Bits 3 and 4 are the direct inputs from the AFE current monitoring circuitry. Bit 5: Test Pulser Power (bit 2 of the General Register/Controls - Addr X0) Bit 6: Front Event Enable (bit 0 of the Front Detector Enables Register - Addr X2) Bit 7: Rear Event Enable (bit 0 of the Rear Detector Enables Register - Addr X4) Bits 15:8 - a readback of the Global Enables/ Controls Register, located at Address X1	DAC Programming Register Bit 11- Bit 0 programs the DAC data word. This word is latched following any DAC write cycle, holding the DAC data bus the last programmed value. Bits 14 - 12 control the 8408, a quad DAC used to drive the AFE threshold settings. Bit allocation: Bit 12: Creates Data Strobe 0 Bit 13: Creates Data Strobe 1 Bit 14: Drives SELA Bit 15: Creates Write strobe to Pulser DAC (an AD7545) Data and Write strobes (300ns) are generated by DIF sequential logic, based on the state of bits 12, 13 and 15, following any write to address XC. SELA is latched in the same manner as the DAC data word. All signals are passed onto the DACs without a change in polarity. NOTE: Data and write strobes are active low. For further information, see DAC specifications.
XD	Not used	Not used
XE - XF	Not used	Not used
F0		Analog Mux Select Bits 7-4: CARD-ID Bit 3: Analog Mux Select (1 -> set AMUXENB1) (0 -> set AMUXENB0) Bits 2-0: Analog Mux Addr If data bits 7-4 match CARD-ID, the DIF generates an analog mux select.