BCF Description and Functional Specification

Revision B
29 February 2000

HSI_IDPU_014D

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References.

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HESSI IDPU Bus Controller FPGA Specification, D.W. Curtis, 98-Jun-15

HESSI IDPU Processor Specification, D.W. Curtis, 98-Jul-2

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HESSI IDPU Detector Interface FPGA Specification, D.W. Curtis, 98-3-31

DIF Description and Functional Specification, D. Gordon, Rev. C, 29 February 2000

PFF Description and Functional Specification, D. Gordon, Rev. B, 29 February 2000

MUEUART, D.W. Curtis, 3-10-1992

Revision History

Revision Number	Date	Change Summary
0.1	July 6,1998	Initial Draft
0.2	April 23, 1999	Set Watchdog reset timeout to ~3 seconds Added ADC Latchup Protection & Diagnostic Register Added Transfer Request Mask Register General Updates
A	August 18, 1999	Formal Release - Corresponds to BCF Rev. 5
B	February 29, 2000	Revision since August, 1999: Includes extension in length of IDPU bus cycles Corresponds to BCF Rev. 8

Introduction

The BCF (Bus Controller FPGA) is a component of the Data Controller Board of the HESSI IDPU. Housed in an Actel the Actel 14100A (10K gates), it includes logic interfacing the CPU to its various subsystems (memory, IDPU bus, registers), particle detector counters, an IDPU bus controller, arbitor, and miscellaneous functions. A block diagram appears below:

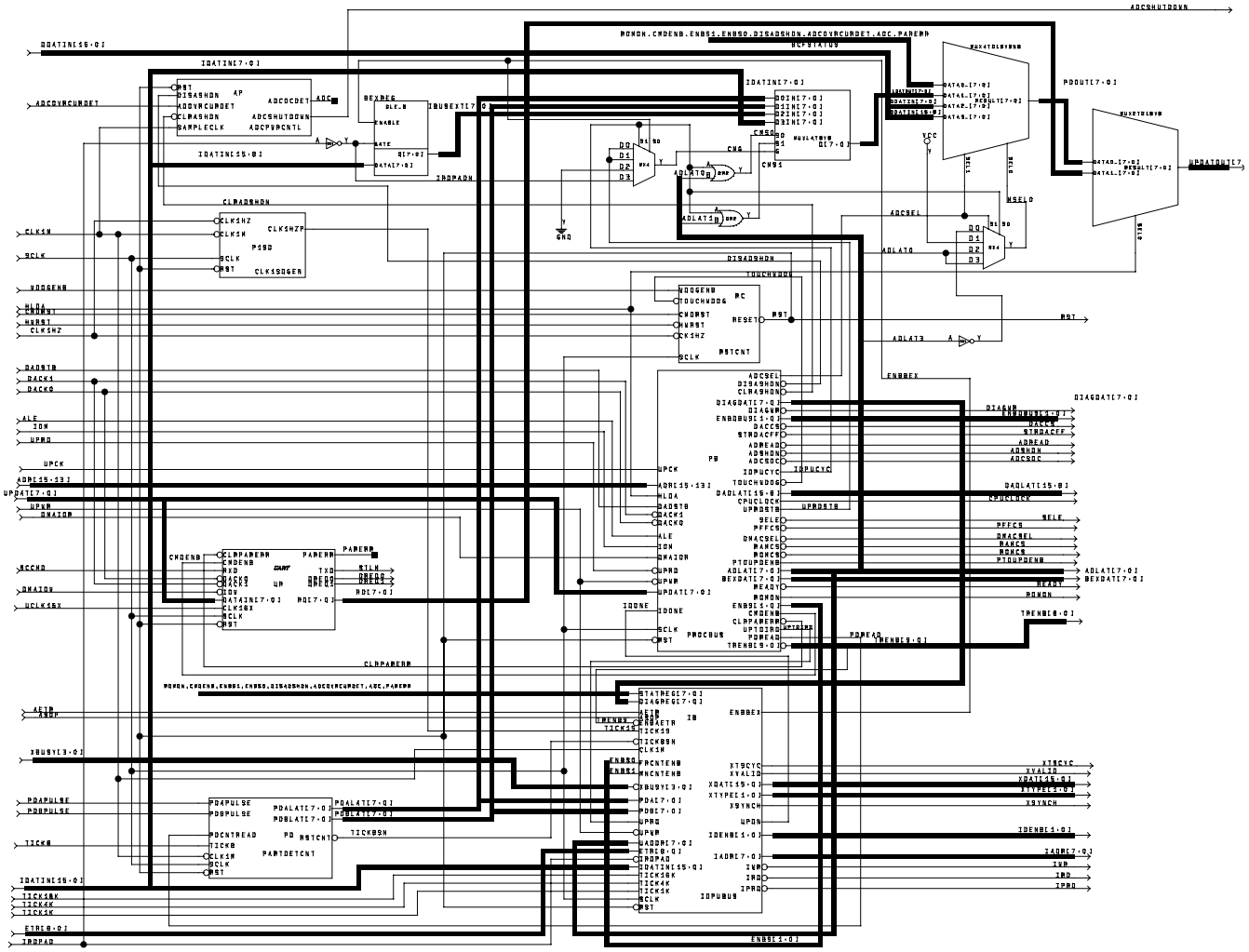


FIGURE 1. BCF - Overall Block Diagram

The BCF receives master timing signals from the PFF, and conditions them to provide timing pulses required by the various BCF modules. Components descriptions follow:

1.0 Reset Controller

The reset controller (RSTCNT) is shown on the right side of the BCF Overall Block Diagram, directly above the CPU Interface (PROCBUS). Reset sources include: a power-on hardware timed reset, a S/C bilevel commanded reset and a watchdog reset.

The power-on reset, set by an external RC time constant (see HESSI IDPU Processor Specification), insures that the power supply is stable before the deassertion of reset. It is normally high, asserted low at power-up.

The S/C bilevel reset is a normally high low-going pulse with a duration of 100ms as it arrives at the BCF FPGA after one inversion on the Data Controller Board. See the IDPU ICD for a description of this signal and its receiver circuitry.

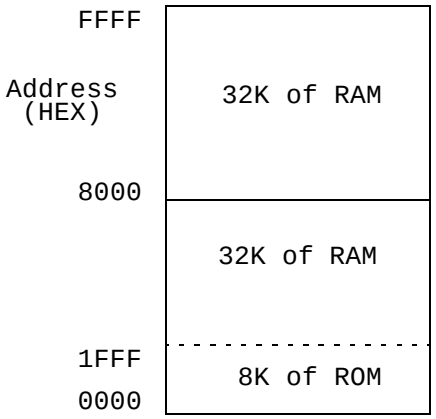
Watchdog reset is initiated by a timer internal to the BCF. The watchdog reset module generates a reset pulse after 3 seconds (or more precisely, 3 ticks of the S/C 1 Hz clock), if the CPU has not written to the watchdog reset register (see “Bus Registers” on page 5). The width of the watchdog reset, ~5 microseconds, is timed to exceed the 8085 CPU “warm reset” minimum pulse width requirement. A watchdog enable is provided as an input pin to the BCF. (The enable can be pulled-up for normal operation and jumpered to ground when a watchdog disable is needed.)

All reset sources are ORed together to generate the overall IDPU reset line (active low). This signal resets the 8085 CPU resident on the data controller board, the BCF itself and other FPGAs resident on the data controller board, and all the detector interface boards.

2.0 CPU Bus Control

The CPU bus control and 8085 control circuitry resides in the PROCBUS module shown in Figure 1. (8085 interrupt control latching/logic is contained in the PFF.) The BCF decodes and latches the 8085 address as follows:

For memory accesses (when the 8085 signal IOM=0), the ROM and RAM are mapped concurrently to address zero. It results in the following memory map:



The ROM appears only once (does not “wrap”) within the 32K memory space allotment. The RAM aliases 2X within the 64K processor memory space. When the ROM is powered on (default at reset) all reads between addresses 0-1FFF Hex access ROM, but all writes access RAM. (With the ROM powered on, the RAM can still be read at address 8000 Hex.) When the ROM is powered off (controlled by a register bit set by the CPU, described in Section 2.1) all reads and writes access RAM only.

The processor read and write signals, also driven by the 82C37 when DMA is active, directly connect to the RAM and ROM. RAM chip select (RAMCS) is asserted by the BCF in either of two cases. If one of the DMA acknowledge lines (DACK0 or DACK1) is asserted, indicating that the 82C37 is bus master, the BCF generates a RAM chip select during memory transactions (IOM=0). When HLDA is deasserted, indicating that the 8085 is bus master, an 8085 RAM address decode bus generates RAM chip select.

The BCF latches the multiplexed address data bus of the 8085 to generate ADLAT[7:0] which can be used to directly drive the 8085 memory address bus. It also latches the upper address bits from the 82C37 during a DMA cycle and outputs DADLAT[15:8] which can also directly drive the 8085 memory address bus. DADLAT is enabled only when HLDA is asserted; ADLAT is enabled only when HLDA is deasserted.

The IO space (when the 8085 signal IOM=1) is divided between Data Controller card subsystems and the IDPU backplane. It is apportioned as follows:

IO Address (Hex)	Selected Subsystems
0-8	Detector Interface Cards
9	Aspect Data Processor
A	Power Controller
B	Bus Controller FPGA (internal registers)
C	Packet Formatter FPGA (internal registers)
D	DMA Controller (82C37)
E	PFF MemoryTest Mode
F	IDPU backplane Broadcast Mode

TABLE 1. IDPU Memory Map

For programming details, see specifications relating to selected subsystems. The Bus Controller registers are described in this document, Section 2.1 below.

2.1 Bus Registers

The BCF contains the following registers, mapped into IO address space as follows:

Address	Read Register	Write Register
B0	Particle Detector Counter - A 8 bit compressed count, latched 8 times/ second. (See Section 6.0)	Power Switches Bit 0: ROM Off setting this bit to zero turns off power to the ROM. It defaults to one at reset
B1	Particle Detector Counter - B 8 bit compressed count, latched 8 times/ second. (See Section 6.0)	Enables/Controls Bit 0: Enable Fast Rate Counters Bit 1: Enable Monitor Rate Counters Bit 2: Uplink Enable - Enable for the command DMA channel. Bit 3: Disable Overcurrent Shutdown - Disables the ADCSHUTDOWN signal. Bits 0 and 1 (when set to one) enable the Fast Rate or Monitor Rate counter packet collection. All Enables default to zero at reset.
B2	Bus Extension Register This register holds the upper 8 bits of data from the last IDPU bus read.	Bus Extension Register This register drives the upper 8 bits of the next IDPU bus write.
B3	Not used	Any write to address B3 touches the watchdog timer (see Section 1.0, “Reset Controller,” on page 2)
B4	ADC Data, lower byte NOTE: the Analog channel must be selected (and IDPU bus broadcast), and an SOC pulse must be issued (at address B5).	ADC Control Bit 0: ADC Shutdown - defaults to zero at reset. (When ADC Shutdown=0, the ADC is in “nap mode”; otherwise, the ADC is ready to convert.)
B5	ADC Data, upper byte	Any write to address B5 pulses the SOC line of the ADC, causing a conversion. Data can subsequently be read back at addresses B4 and B5.
B6	undefined	DAC Writes byte to Particle Detector Control DAC.
B7	undefined	Diagnostic Register Bits 7:0 of the CPU data bus are strobed into two separate latches, one is external, serving as a debug data bus, and the other is internal to the BCF. The internal diagnostic register is telemetered along with the Monitor Rate Data.

Address	Read Register	Write Register
B8	BCF Status Register Bit 0: Uplink Parity Error Bit 1: ADC Overcurrent Detect (Latched) Bit 2: ADC Overcurrent Signal (Input to BCF, unlatched version direct from analog circuitry.) Bit 3: ADC overcurrent shutdown disable (bit 3 of Enables/Control register) Bit 4: Fast Rate Counters Enable (bit 0 of Enables/Control register) Bit 5: Monitor Rate Counters Enable (bit 1 of Enables/Control register) Bit 6: Uplink Enable - follows bit 2 of Enables/Control register. Bit 7: ROMON - Bit 0 of Power Switch Register The Status register is telemetered along with the Monitor Rate Data.	BCF Pulse Register Bit 0: Clear Uplink Parity Error Bit 1: Clear ADC Shutdown Detect
B9	undefined	Transfer Request Mask Register Low A mask register which defaults to low at reset (all subsystems enabled). Setting any bit in this register disables transfer requests from the corresponding subsystem. Bits 7-0: Correspond directly to ETR[7:0]
BA	undefined	Transfer Request Mask Register High A mask register which defaults to low at reset (all subsystems enabled). Setting any bit in this register disables transfer requests from the corresponding subsystem. Bit 0: ETR8 Bit 1: ADP Transfer Request
BB-BF	undefined	not used

TABLE 2. BCF Internal Register Memory Map

3.0 ADC Latchup Protection

An active high input (ADCOVRCURDET), driven by the ADC power control circuitry, indicates an ADC latchup. If the Overcurrent Shutdown is enabled (Register B1, Bit 3), a high level on ADCOVRCURDET causes an assertion of ADCSHUTDOWN, which shuts down power to the ADC and sets an overcurrent detect status register bit. This status bit (readable at register B8, bit 1) is latched in until explicitly cleared by the CPU via the BCF Pulse Register (register B8, bit 1). The real-time signal from the analog circuitry is also available as status (register B8, bit 2).

Overcurrent Shutdown Disable and Status (latched) are all cleared by RESET. ADCSHUTDOWN is preset (jammed high in order to disable the ADC) by RESET.

The shutdown can only be disabled by the CPU explicitly setting the Disable Overcurrent Shutdown Register bit (register B1, bit 3).

NOTE: The ADC Overcurrent detect status bit will be set even if the Overcurrent Shutdown is disabled; the disable bit inhibits the signal at the final stage, as it is driven out to the ADC power control circuitry.

4.0 UART

The UART is a standard 8-bit bidirectional UART using one start bit (asserted low), 8 data bits followed by one parity bit. Parity is defined as "even" in the following manner: the eight data bits plus one parity bit are forced by the parity bit to incorporate an even number of ones. The parity bit is followed by one stop bit (active high). (The serial lines follow the protocol described in the HESSI IDPU ICD.)

The UART is based on an Actel 1020 macro which has been adapted from a previous project (see MUEART description). The baud rate is set by SCLK divided by 16, generating a 16X clock (UCLK) of 625KHz. UCLK is routed to an internal high speed clock net, minimizing skew at the clock inputs of the UART shift registers. The resulting bit rate is actually 39.0625 KHz, giving approximately 1.7% error per bit from the specified 38.4 Kbaud.

The UART interfaces directly to the 82C37 DMA controller (DMAC): Channel 1 is dedicated to the Commands; Channel 2 to the slow telemetry interface. All DMA control bits are set to the default polarities required by the 82C37 (DACK is active low and DREQ is active high.)

4.1 Command Interface

Upon reception of a data byte, the UART module generates a DREQ0 if the command I/F is enabled via the Uplink Enable, bit 2 of the Enables/Controls Register. If DMA is enabled, the DMAC will request the bus from the 8085, and generate DACK0 upon receiving a bus grant. It will then read out the UART and write the data byte into a pre-programmed memory location.

If a command parity error is detected, the BCF sets a latch (UPLINK PARITY ERROR) which is readable and resettable by the 8085. (UPLINK PARITY ERROR does not affect the state-machine operation; it just informs the processor that an error has been detected.)

4.2 Telemetry Interface

The telemetry interface operates much like the command interface in reverse. If the transmitter is empty the BCF asserts DREQ1. After the 8085 initializes DMA channel 1, the DMAC requests the bus from the 8085, and generates DACK1 which transfers a byte from a preprogrammed memory location into the transmit latch. Once the byte has been transferred from the holding register into the UART transmit shift register, DREQ1 asserts again, causing the next DMA transfer. Parity is computed by the BCF UART and shifted out following data bit 7.

5.0 IDPU Bus Control

The IDPU bus controller, shown in Figure 2, performs arbitration and timing control for the IDPU bus, a 16-bit data, 8-bit address, bi-directional bus. The BCF is the IDPU bus master, driving address and control strobes continuously, while arbitrating between the various IDPU bus requestors.

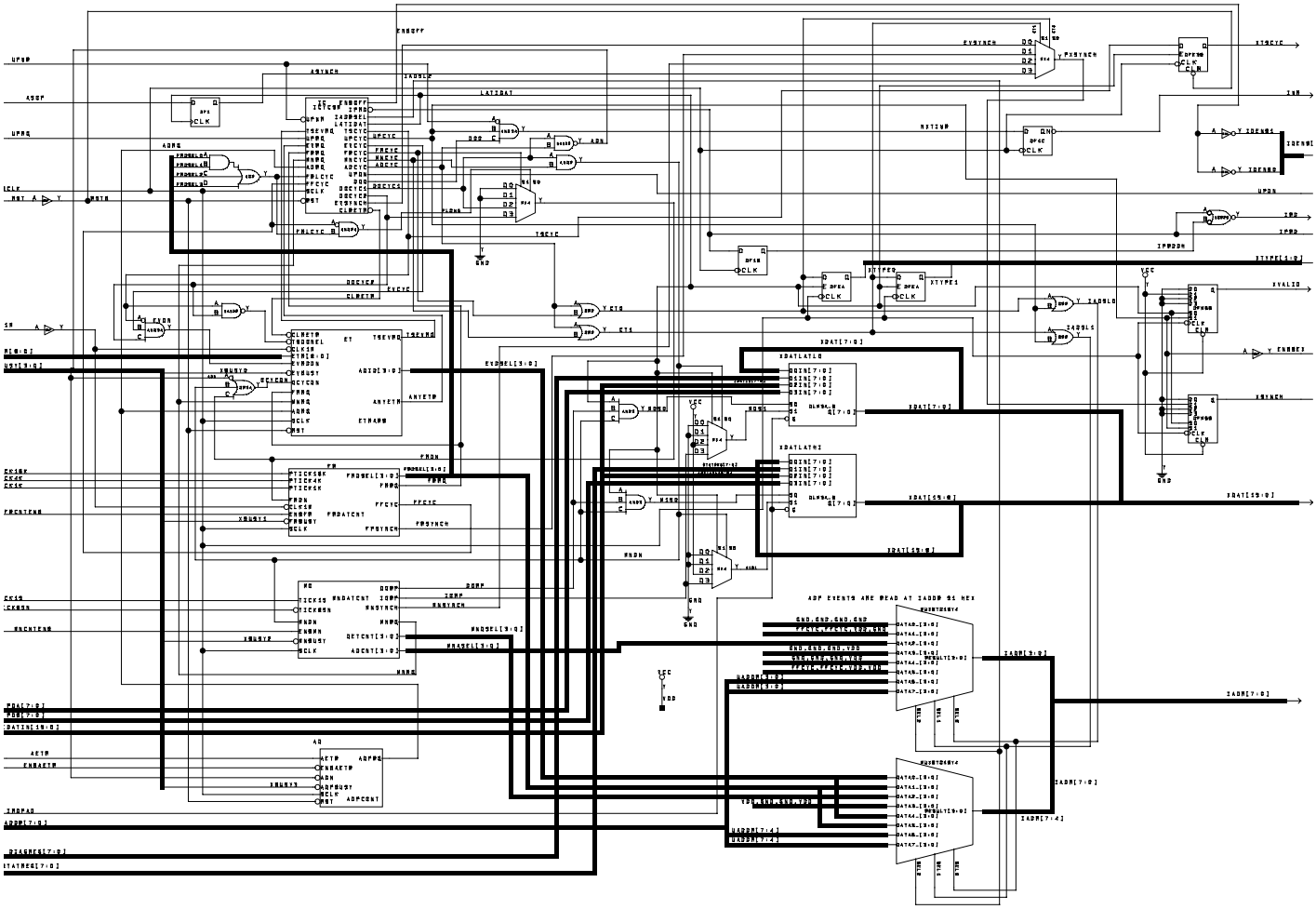


FIGURE 2. IDPU Bus Controller

Shown on the upper left is the ICYCLE state machine/IDPU bus arbitor. Requests are processed and IDPU bus cycles are timed by this module. The priority ordering is as follows:

IDPU Bus Requestor	IDPU Cycle	Cycle Length	Comments
Priority 1: 8085	UPCYC	300 ns	Highest Priority, but infrequent. The only IDPU bus subsystem which can perform writes, the 8085 can randomly read/write all IDPU registers (see Table 1 on page 4; addresses 0X-AX hex and address FX hex cause the processor bus controller to request an IDPU cycle).
Priority 2: DIFs	EVCYC	600 ns (a 32-bit read requires two back to back IDPU cycles)	On demand event processing from all 9 DIFs; priority amongst the DIFs is cycled. One out of 10 accesses gives preference to the lower priority contenders, i.e. the counters and ADP.
Priority 3: Fast Rate Counters	FRCYC	300 ns or 600 ns (either 16 bit or 32 bit reads required)	Timed by TMCNT, DIFs are read out at various rates: 16KHz, 4KHz and 1KHz. Frequency and number of bytes vary according to DIF-CARD-ID.
Priority 4: Monitor Rate Counters	MNCYC	300 ns	Particle Detector counters read out 8X/second (internal to the BCF, these accesses do actually create No-op IDPU cycles), and 40 DIF register accesses once/second.
Priority 5: Aspect Data Processor	ADCYC	300 ns	On demand packet readout. The ADP drives its own ETR and SOP (start of packet) signals.

TABLE 3. IDPU Cycle Types

Worst case data access for the CPU is approximately 1μs, requiring a wait state in order to insure that IDPU data returned on a read cycle is valid when the 8085 samples it. This wait state is inserted by the BCF only during off-board (IDPU) accesses. Figure 3, below, shows a 8085 to IDPU write cycle followed by a read cycle. (UPWR and UPRD are the 8085's WRITE and READ; ALE is the 8085's address latch enable.)

IDPU bus address is generated by the muxes shown in the lower right of Figure 2. The upper nibble selects the card, while the lower nibble selects the register on the addressed card. Each DIF readout subsystem (described in following sections) keeps track of its own card addresses; the IDPU cycle type steers the appropriate address out onto the bus. During UPCYCs, the 8085 busses are fed directly into the IDPU bus. A bus extension register (see Section 2.1) drives the upper half of IDPU data and latches these 8-bits during a read cycle. (NOTE: the Bus Extension read and write registers are separate. Data written by the CPU does not read back, it just drives the

IDPU bus. Similarly, data latched during an IDPU read, does not alter data last written by the CPU.)

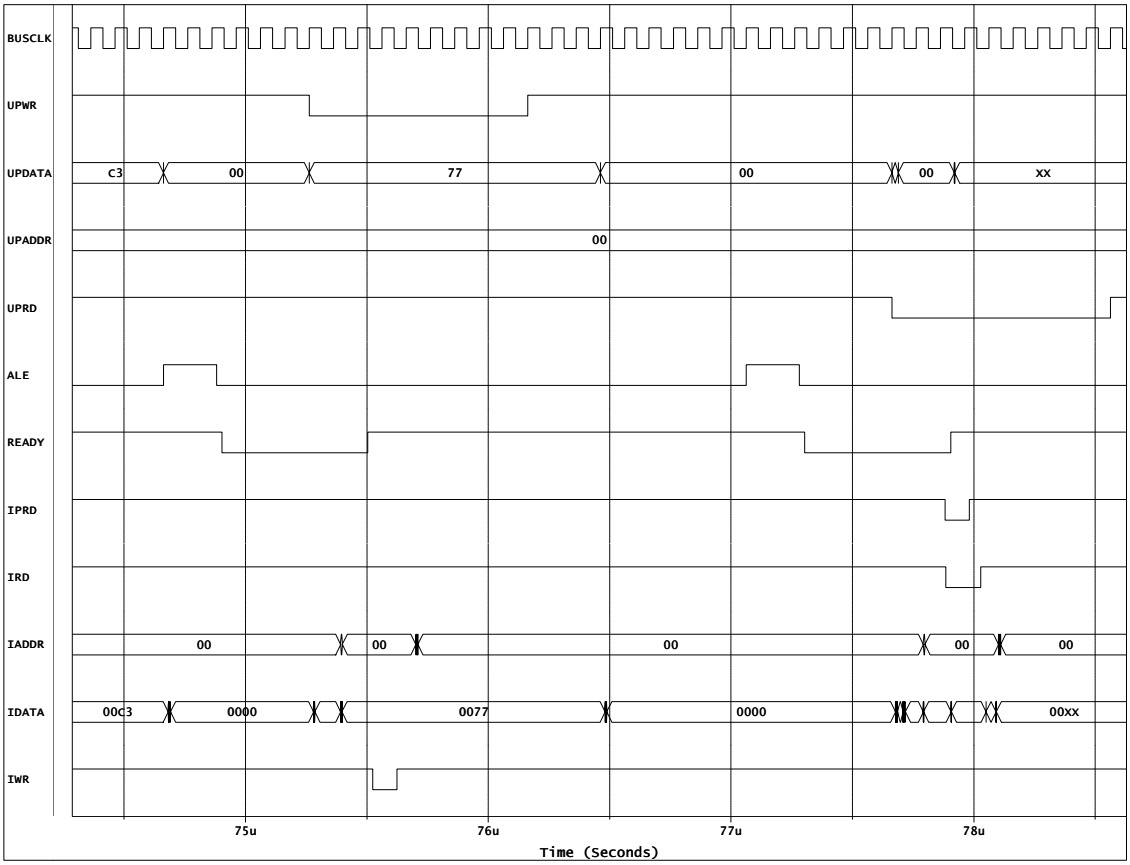


FIGURE 3. 8085 IDPU Bus Cycles

A “dead” zone of one-clock is inherent in each subsystem’s bus grant. (This is due to the hand-shake between the IDPU bus controller and the individual subsystem’s controllers.) Therefore back-to-back ADP cycles will occur at a frequency of 400ns on the IDPU bus. (DIFs of differing IDs are not subject to the “dead” zone; the 100ns recovery, however, does apply to back-to-back transfers from one DIF.)

5.1 ETR Arbitration

ETR (event transfer requests) are driven by all 9 DIFs as ETR[8:0]. The ETR[8:0] is routed through the module IPSEL, which contains 9 unique priority encoders.

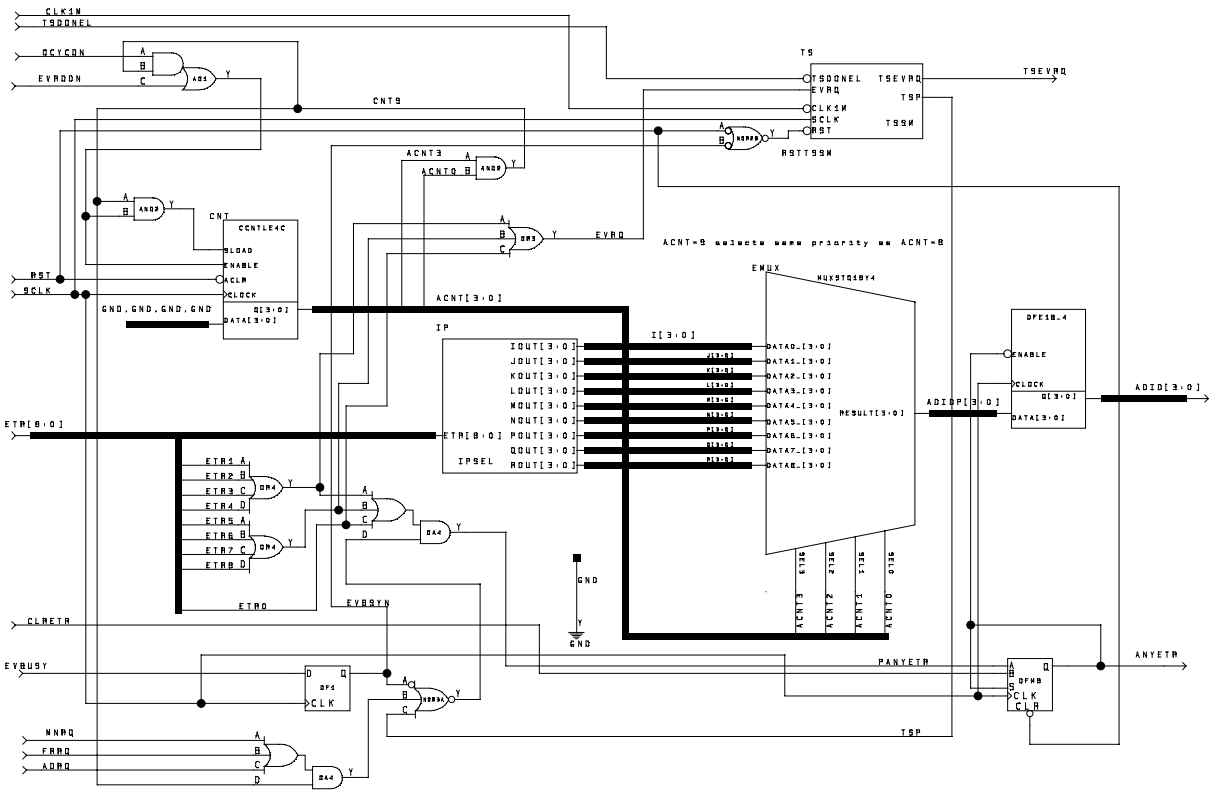


FIGURE 4. ETR Arbitration Module

Not shown in Figure 4, but contained in the top-level schematic, are the ETR “masks”. Each ETR, as well as the ADP transfer request, can be individually disabled via the transfer request bit mask registers (see Table 2 on page 6).

The priority encoders output a four bit binary code, selecting one of the nine DIF CARD-IDs. A counter, clocked by a cycle termination signal, circulates through the nine priority encoders via a 10 to 1 mux shown at the right of Figure 4. The 10th count is reserved for the lower priority IDPU bus contenders, whose requests are shown on the lower left of the figure. If there are no other requests, the last IPSEL priority encoder (ROUT[3:0]) is reused; then the counter clocks back to select address zero (IOUT[3:0]) once more.

Event Synch pulses forwarded to the PFF are generated for the first half of each 32-bit cycle (two IDPU reads). This function is tracked by the overall IDPU cycle state machine (ICYCSM), mentioned in the above section. Upon termination of the second read, ICYCSM asserts EVDN, which clocks the ETR arbitration counter.

The PFF BUSY signal (EVBUSY) suppresses the ANYETR output, effectively shutting down DIF data collection.

The upper right hand section of Figure 4 shows the module “TS” state machine which controls the insertion of “time-stamp” events. A time-stamp event is generated if there is a delay of >1ms between two DIF ETRs. It is inserted as a result of the arrival of the first ETR following the 1ms gap, preceeding ETR servicing. The BCF asserts a signal called “TSCYC” which informs the PFF that the current bus transfer is a TimeStamp event. The PFF inserts the actual time-stamp as the event is written into packet memory. The actual event (which caused the timestamp) follows.

5.2 Fast Rate Counter Controller

The Fast Rate Counter subsystem keeps track of time by monitoring the BCF overall timebase counter (TMCNT). It pays attention to three types of “TICKS”: TICK16K, TICK4K and TICK1K. The TICKS are conditioned by FRTCKDET using base timing signals received from the PFF. The Fast Rate cycle controller reads DIF ID’s 0,1 and 2 for all ticks, DIF ID’s 0-5 for TICK4K all DIF IDs (0-8) for TICK1K. FRDSEL[3:0] indicates the currently selected DIF The lower nibble, hardwired into the IDPU address generator mux, is selected by ICYCSM.

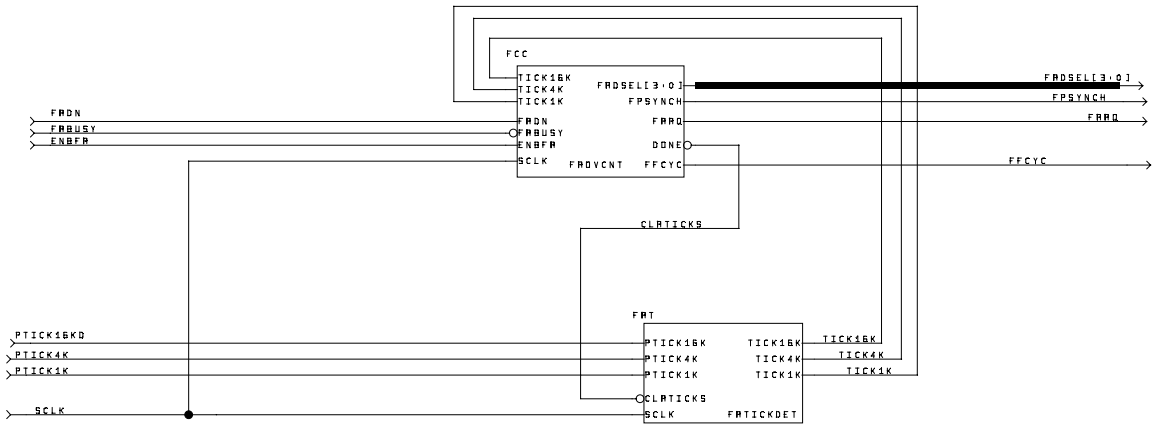


FIGURE 5. Fast Rate Counter Controller

Readout sequences are ordered in accordance with the Fast Rate Packet 180-byte cycle format described in the HESSI Telemetry Formats document. A synch pulse is generated by the first cycle following a TICK1K readout sequence. To fill the last 12 words at the end of each Fast Rate “Cycle” (see HESSI IDPU Telemetry Formats), the BCF reads the DIF status registers sequentially (DIF-IDs 0-8 and then 0,1 and 2 again) and inserts this information into the Fast Rate Telemetry stream.

Either deassertion of the enable bit, programmed by the 8085 via a BCF register (see Section 2.1) or assertion of the XBUSY (FRBUSY) signal driven by the PFF can shut-down the Fast Rate Counter Controller data collection.

5.3 Monitor Rate Counter Controller

The monitor rate counter controller looks for the 1 second tick (TICK1S), and uses this to tack a synch pulse onto the next readout. It then looks for TICK8S, generated by the Particle Detector Subsystem (see Section 6.0).

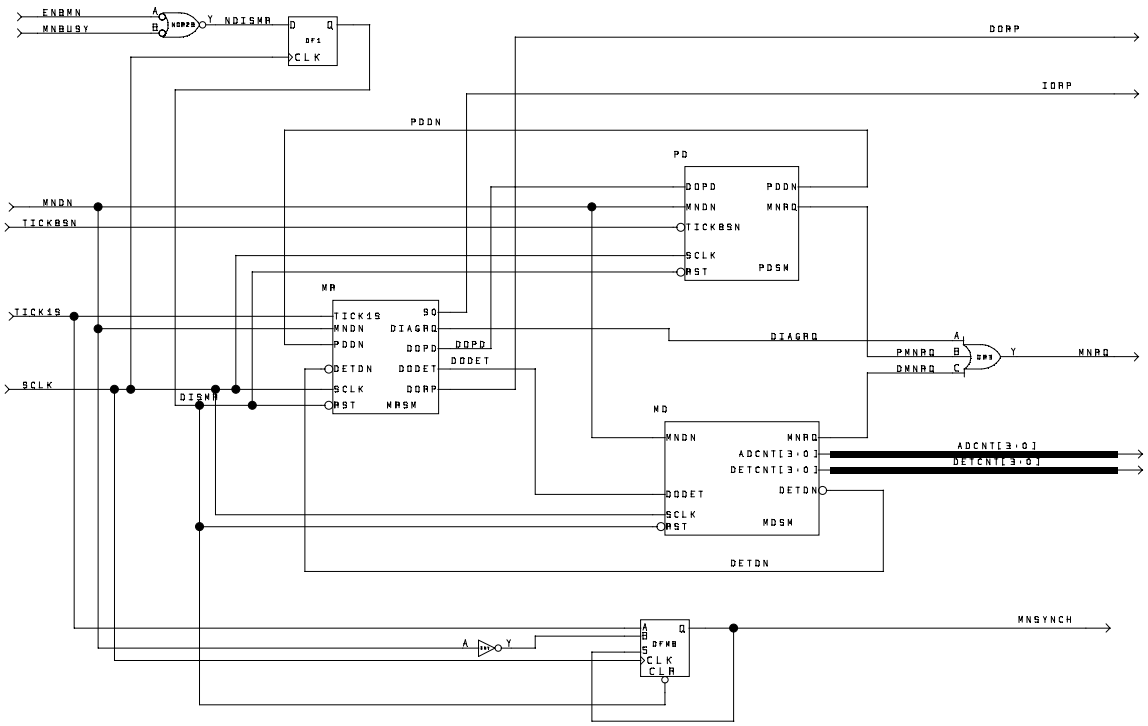


FIGURE 6. Monitor Rate Counter Controller

MRSM counts the number of data collection cycles (just Particle Detector readouts) due to TICK8S. Upon detection of the 8th readout, it activates the MDSM, which reads out all the DIF monitor rate counters according to the format outlined in the Monitor Rate Packet 108-byte Cycle Format described in the HESSI Telemetry Format document.

Data is accumulated prior to latching, so the monitor rate register collection times (starting from the first cycle in a packet), correspond to the packet timestamp as follows:

PD-A 0	
PD-B 0	accumulated 1/8 second prior to timestamp
PD-A 1	
PD-B 1	accumulated at timestamp to 1/8 second after the timestamp
...	
PD-A 7	
PD-B 7	accumulated between 6/8 and 7/8 of the second
DIF data	accumulated in the second prior to timestamp

The controller writes the last bytes (106 -107) of the Monitor Rate cycle with BCF related diagnostic data. Byte 106 contains the Diagnostic Register, and bit 107 contains the BCF status register. (See HESSI Telemetry Formats for a definition of the bytes in the Monitor Rate Cycle.)

Either deassertion of the enable bit, programmed by the 8085 via a BCF register (see Section 2.1) or assertion of the XBUSY (MNBUSY) signal driven by the PFF can shut-down the Monitor Rate Counter Controller data collection.

5.4 Aspect Data Processor Interface

The Aspect Data Processor (ADP) interface transfers data in 16-bit units from the IDPU bus to the Packet Formatter bus. Each ADP-ETR causes one 16-bit IDPU read. A synch is generated based on the ADPSOP signal in the following manner: ADPSOP asserts (active high) as a result of an IDPU read of the last word of a packet. It then deasserts as a result of an IDPU read of the first word of the next packet.

ADP data collection can be supressed by the assertion of XBUSY3 (ADPBUSY), by the PFF. ADP-ETR can also be masked via the ETR Mask Register (see Table 2 on page 6).

5.5 Packet Formatter Interface

All IDPU bus cycles except those initiated by the 8085 create packet formatter transfer strobes. Data is transferred from the BCF to the PFF (Packet Formatter FPGA) via 16-bit unidirectional bus. The interface includes the following signals:

XVALID	strobe indicating a valid IDPU to PFF data transfer
XDATA[15:0]	16 bits of data being transferred
XSYNCH	start of data unit (cycle for rates, packet for ADP, event word for DIFs)
XTYPE[1:0]	type of data being transferred
XTSCYC	indicates a time-stamp cycle (only valid during DIF Event cycles)

XTYPE is broken down as follows:

CYCLE TYPE	XTYPE CODE
DIF Event Cycle	0
Fast Rate Cycle	1
Monitor Rate Cycle	2
ADP Cycle	3

TABLE 4. Packet Formatter Cycle Types

For each cycle type, the PFF can assert a BUSY signal (XBUSY[3:0]) which stops all IDPU accesses for the selected subsystem.

The BCF generates SYNCHs at the appropriate intervals and orders counter data as specified by the HESSI Telemetry Formats document. It does not attempt to eliminate partial packets or begin data collection based on the cycle/packet boundaries. This task is done by the PFF.

6.0 Particle Detector Counters

The particle detector counters are two 20-bit counters (implemented as ripple counters) which are clocked by input pulses. The output of each counter is routed to a latch after compression via a logarithmic compression module (LOGCOMP). (The specification for LOGCOMP follows Table 3.1-2 of the HESSI IDPU Detector Interface FPGA Specification.)

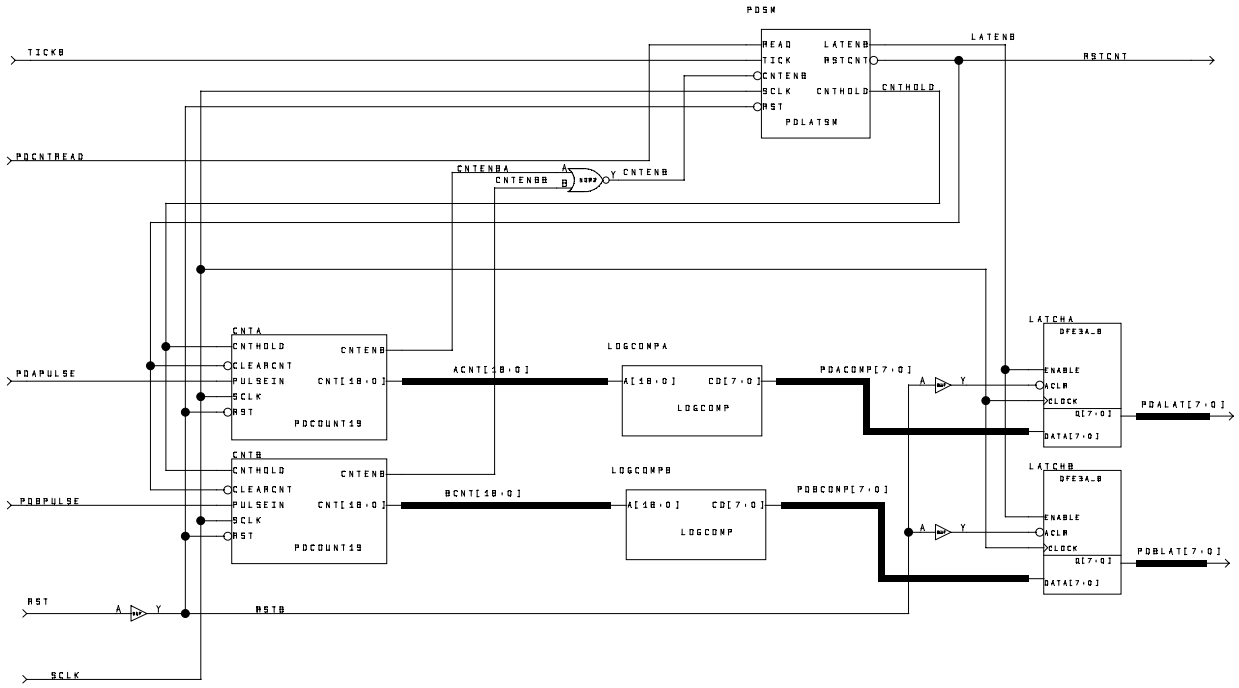


FIGURE 7. Particle Detector Counters

The subsystem operates as follows: The two pulses (PDAPULSE and PDBPULSE) are steered to the appropriate ripple counter. The PFF provides the $^1/_8$ second pulses (TICK8) which cause the counter data to be readout, compressed and latched. Counter data is steered through 19:8 bit log compression modules (LOGCOMP) into 8 bit registers. Following latching, the control logic resets the counters and forwards the $^1/_8$ second pulse to the IDPU Bus Controller, Monitor Rate Counter module, where it initiates a IDPU to PFF data transfer (see Section 5.3).