HESSI IDPU DIB
Proposed Change to Live Time Measurement and Pile-up Rejection

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1. The Current Design

The live time circuit as implemented on the DIBs is flawed. Dead time is measured as 16µs following the most recent (positive) crossing of the slow channel discriminator. But there is no mechanism to veto subsequent events that occur in this window for events below the fast discriminator level. Above the fast discriminator level, there is pile-up vetoing of events that can veto both events if the occur before the conversion pulse, and only the second if it occurs after the conversion pulse but before the end of the pile-up window (about 9µs). The measured dead time has very little relationship with the actual detector dead time.

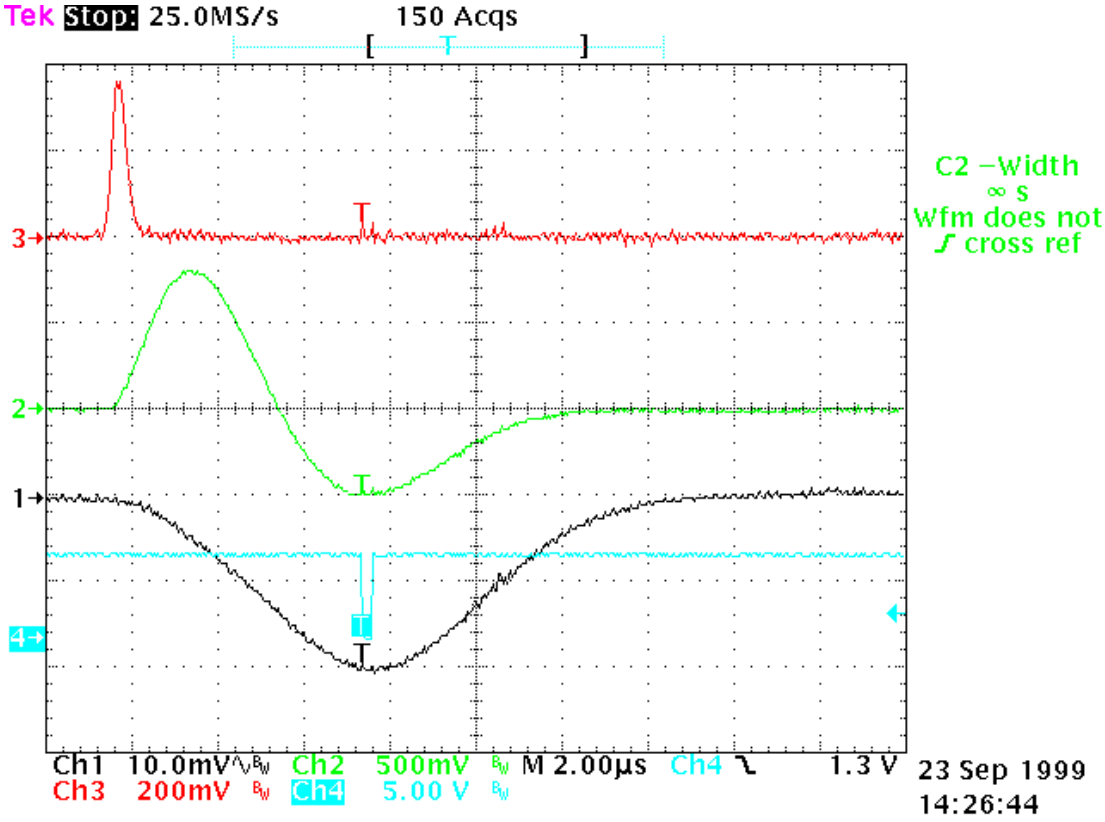

Figure 1. Source Signals

Figure 1 shows a scope snapshot of the typical signals associated with an event. The top signal (Trace 3) is the Fast discriminator input. The next signal (Trace 2) is the Slow discriminator input. The next signal (Trace 1) is the signal into the ADC (Ananlog to Digital Converter), and the last signal (Trace 4) is the ADC convert strobe.

2. Issues

For higher energy events (above the fast discriminator), the pile-up circuit works well at eliminating pile-up. A reasonable measure of the dead time for this circuit is the pile-up window, which starts when the fast discriminator threshold is exceeded, and extends 9us after the latest exceedance (retriggerable). The only problem is that the effect of the circuit will need to be modeled to determine the rate correction since two events can produce zero, one, or two measured events depending on how close the events are. At least there is no significant energy dependence provided both events are above the fast discriminator threshold level.

For lower energy pulses (below the fast discriminator threshold level, but above the slow discriminator threshold level), the situation is complicated. There is no reliable way to know if multiple events occur during the pulse shaping time. If a second low energy event occurs during the time that the slow discriminator is still active (typically about 3-4μs), then the slow discriminator will remain active somewhat longer (due to the pile-up of the signals). In this case, the detector is effectively dead while the discriminator is high. If a second event occurs after the discriminator goes inactive, it may or may not cause a re-crossing of the discriminator depending on the relative size of the two pulses (the second pulse must overcome the negative tail of the first). This makes an energy-dependent dead time. To avoid this energy-dependence, it would be better to veto any event that occurs between the time that the slow discriminator goes inactive and some later time when the signal into the discriminator has returned to near zero (about 5us).

Another constraint is that the ADC is shut off when the dead-time signal goes inactive. This should not happen before 3μs after the convert pulse or the measured value will be returned as zero.

One final constraint is that the boards have been fabricated and time is short, so a minimum change to the existing circuit is desirable. Also, there is exactly one spare IC location for any extra logic that is required.

There is no easy solution to the dead time issue. Pile-up rejection of events below the fast discriminator is not possible; the best that can be hoped for is pile up rejection for events above the fast discriminator level, and a measurement of dead time for all events which is sufficiently well understood to be able to correct the events rate accurately.

3. Proposed Solution

I propose changing the dead time measurement, and also adding a veto for low energy events that occur within the dead time window.

The dead time shall be a combination (logical-OR) of the pile-up window and a low-energy event window. The low energy event window shall start when the slow discriminator threshold is crossed, and continue about 5μs after the latest time the slow discriminator goes inactive. Both of these windows are retriggerable, so a second event occurring within the window will stretch the dead time.

The existing pile-up circuit shall be used for fast events, with the associated dead time effects described above. The circuit shall be changed to work with the low energy events as follows: The veto signal generated when a second fast event occurs shall also be set when the ADC conversion pulse fires, so that subsequent fast or slow events shall be vetoed. Also, the veto signal shall continue high until the dead signal (OR of fast and slow dead time) goes inactive (the current circuit resets the veto signal when the pile-up window ends). This means that a long string of events all happening close together (before the dead time for the previous event expires) will cause only the first event to be measured (and not even that one if the fast pile-up circuit is triggered).

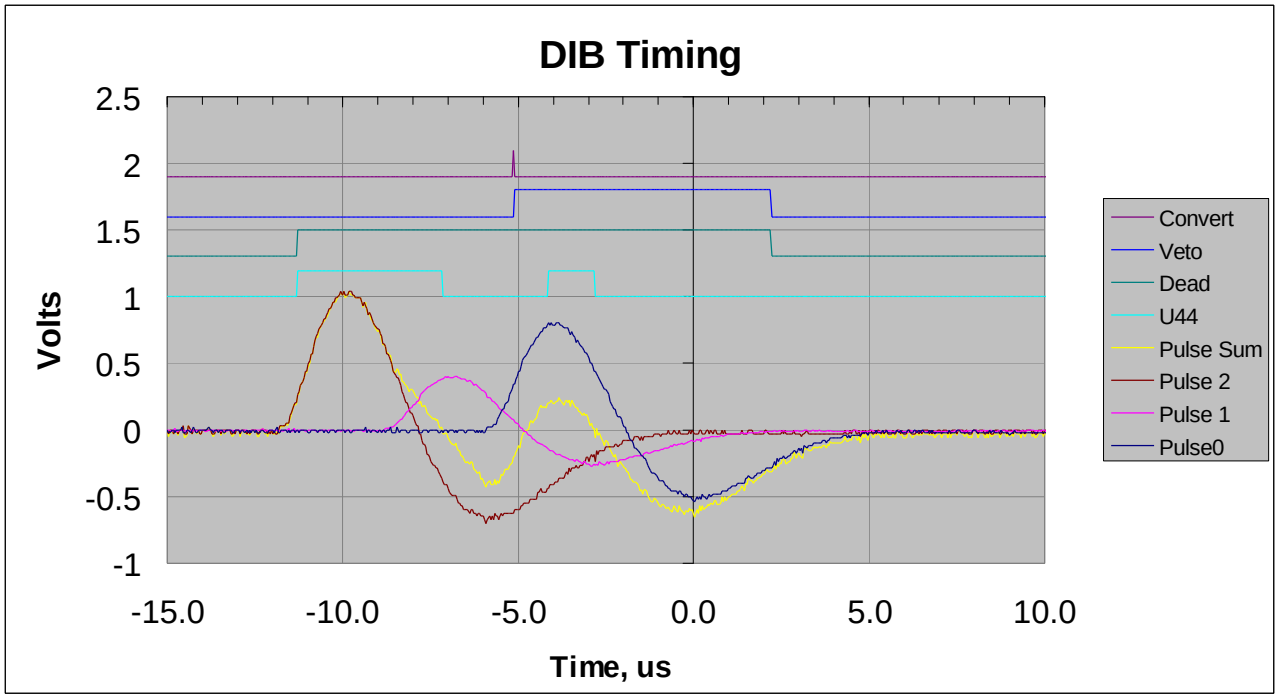

Figure 2 - Slow Discriminator Live Time

Figure 2 shows a simulation of how the proposed system will work with three events into the slow discriminator (ignoring the fast discriminator). The input waveform (captured with an oscilloscope) is replicated with delay and amplitude changes, and the resulting sum is what the discriminator sees. The events occur at 0, 3µs, and 6µs, and have amplitudes 1.3, 0.5, and 1. The first trace above the pulse waveforms (U44) is the output of the slow discriminator. The threshold is set to 0.2V on this scale. Note that the second event does not trigger the discriminator. The next waveform up shows the dead time signal, which will be measured. The next signal up is the veto signal that causes subsequent events to be rejected. The top trace is the ADC convert pulse, showing a single converted event.

If a low energy event (below the fast discriminator threshold) is followed by a high energy event (above the fast discriminator threshold), or vice-versa, the first event will

not be rejected, but the second will if it occurs before the dead time expires. The event energy measurement is likely to be piled-up if the second event occurs before the ADC convert strobe. The circuit acts the same as it does for two low energy events. Pile-up rejection, and the possibility of no conversions, happens only for two high energy events.

This fix can be implemented on the front segment using the available resources on the DIB board (and adding one IC to the spare socket). For the rear segment, I propose using the fast event pile-up for dead time measurement, but making no other change. So long as the fast and slow discriminators are set to the same energy, this should work correctly. If the slow threshold is set below the fast threshold, there will be no dead time measured for events below the fast threshold. If this is not acceptable, the same fix to the rear segment can be made to the rear segment, but it will be more difficult (another IC will have to be added somewhere).

4. The Details

The raw signals that are used in live time and pile up rejection are slow and fast discriminator inputs as shown in Figure 1. The proposed solution is shown in a block diagrams in Figure 3 and 4.

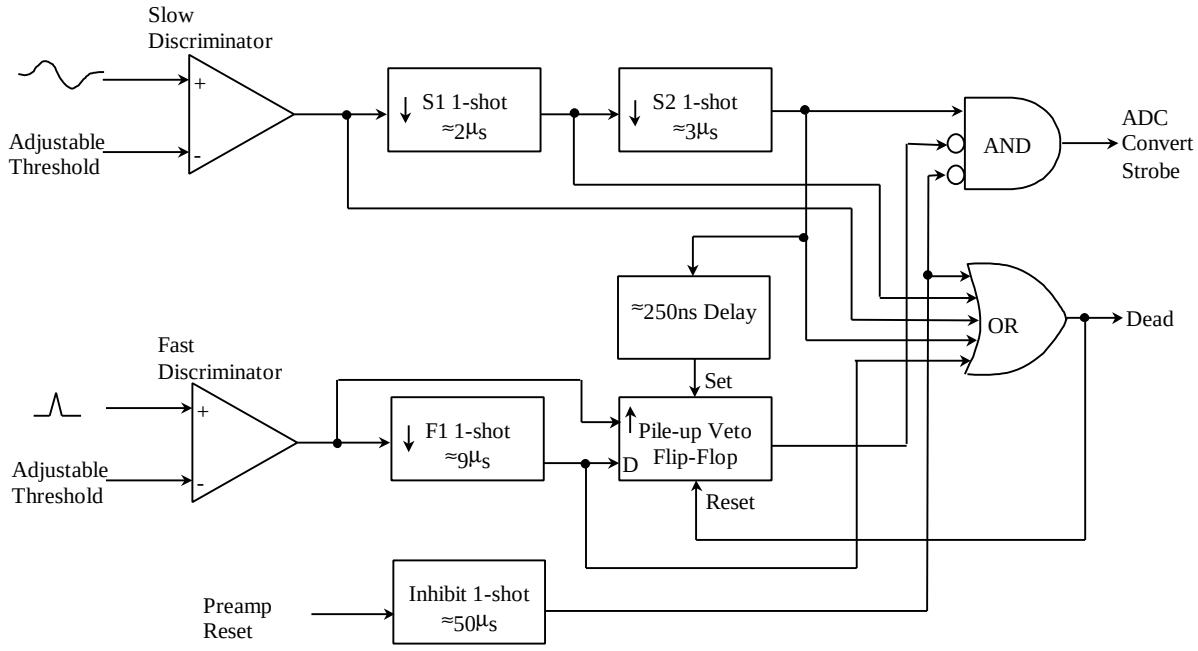

Figure 3 - Front Segment Block Diagram

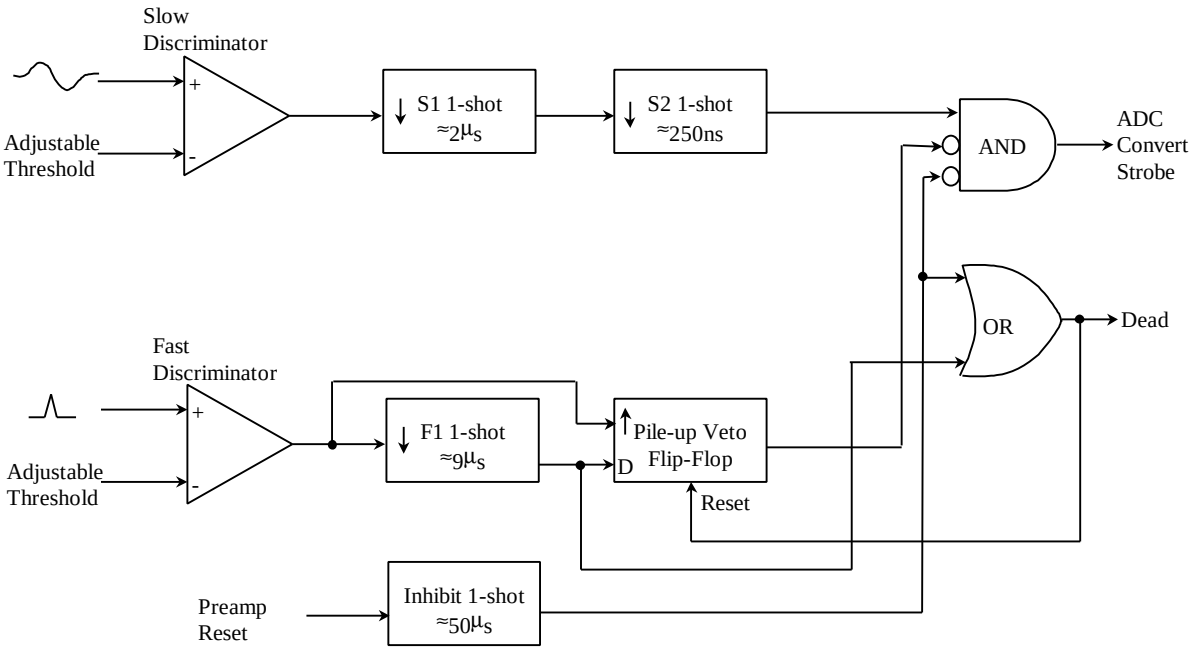

Figure 4 - Rear Segment Block Diagram

4.1. *Fast Discriminator*

The fast discriminator input is a symmetric triangular pulse proportional in height to the energy of the photon, and about 800ns in width at the base. The Fast discriminator goes active when the fast discriminator input exceeds the (programmable) fast discriminator threshold, and goes inactive when it the input falls back below the threshold. The width of the fast discriminator output increases as the pulse height increases, and goes to almost zero when the pulse just exceeds the threshold (a small amount of AC hysteresis limits this shortest pulse out to about 50ns). Note that there is some energy dependence to the exact timing of the edges of the fast discriminator output; to first order, the center of the output pulse should be energy-independent.

The fast discriminator threshold shall be set somewhat above the noise level, somewhere around 15keV.

4.2. *Slow Discriminator*

The slow discriminator input is a differentiated version of an intermediate stage of the pulse shaping. The pulse shape is energy independent, but the pulse height is proportional to the photon energy. If multiple photons come within the pulse shape time, their pulse responses will be added together as shown in Figure 2. The slow discriminator goes active when the slow discriminator input exceeds the (programmable) threshold, and goes inactive when the signal crosses zero. The zero-crossing detect is important since its timing is pulse-height independent. The ADC convert strobe is a

fixed delay following the zero-crossing. The timing of the front edge of the slow discriminator output will vary with the energy of the photon.

The slow discriminator threshold shall also be set some slightly above the noise level. Since the integration time is longer for the slow discriminator input signal than for the fast discriminator input signal, the noise level should be proportionally lower, perhaps around 3-4keV.

4.3. *ADC Sampling*

The ADC is sampled a fixed delay time (about 2µs) after the zero crossing signal generated by the back-edge slow discriminator. This delay is generated by a "1-shot" called P1 that goes active when the Slow Discriminator goes inactive, stays active a fixed time (about 2µs, set during board test to match the peaking time of the ADC input signal), and then goes inactive. S1 is followed by a second 1-shot, S2, originally designed to generate the short (200ns) convert strobe for the ADC. S2 goes active when S1 goes inactive, and stays active a fixed time interval. The ADC starts conversion when this signal goes active. The ADC requires that this signal stay active at least 40ns, and it is recommended that it stays active no longer than 500ns to avoid effecting the conversion. Both S1 and S2 are edge-sensitive and retriggerable, meaning that if the input goes from active to inactive again during the time that the unit is active, the unit will stay active for the designated time interval after this second event.

The ADC conversion signal is inhibited for a short interval after a preamp reset has occurred to give time for the signal string to settle.

4.4. *ADC Conversion Window*

The ADC is power-strobed to save energy. It is in 'nap mode' between conversions. The slow discriminator output signal is used to wake up the ADC (when the signal goes active). The ADC continues to stay awake until the dead time signal into the digital electronics goes inactive; the logic then puts the ADC back into nap mode. This puts a constraint on the dead time signal that it should not go inactive before the conversion is complete (about 2.5µs after the conversion strobe).

4.5. *Pile-up Circuit*

The pile-up circuit is designed to veto events that occur so close together that their pulse shapes into the ADC overlap at the time of the ADC convert strobe. This circuit requires advance knowledge that an event has happened, and so is based on the fast discriminator signal. This means that it does not work for events below the fast discriminator threshold.

The fast discriminator is fed to another one-shot, F1, which is set to about 9µs. Note that F1 is activated when the fast discriminator goes inactive. A pulse occurring before this time would be 'piled-up' with the preceding pulse, causing a mis-measurement of the first event and/or the second events energy. Should the fast discriminator go active a second time while F1 is active, the ADC convert strobe is disabled. The ADC convert disable stays active until the dead time signal goes inactive (see below). Since this can happen

before or after the convert strobe for the first event, you can get zero, one, or two events measured for two input events depending on how close they come together.

There is a short interval before F1 is activated during which two events will be counted as one; this is unavoidable, but kept as short as possible. This interval is approximately equal to the fast discriminator input pulse time (800ns), but has some energy dependence (pulses just exceeding the threshold can be detected closer together than pulses much greater that the threshold, since the signal must return back below the threshold and come back up again to be detected).

Pulses occurring between the time F1 goes active and the time of the ADC convert strobe for the first event shall cause both events to be vetoed.

Pulses occurring after the ADC convert strobe for the first event, but before F1 goes inactive, will cause only the second event to be vetoed.

F1 is also edge-sensitive and retriggerable, so that it will continue active for the set time following the most recent fast discriminator pulse.

4.6. *Low Energy Event Veto*

While you can't do pile-up rejection on events that are too low to fire the fast discriminator, you can ensure that a second event will not cause a second conversion if it occurs too close to the first. This provides an energy-independent dead-time for low energy events. Otherwise second events may or may not cause a conversion based on the relative energies and time interval between the two events (see Figure 2). There is no provision for this in the original circuit, but the proposed design achieves this by setting the Veto signal after the ADC convert signal. Any subsequent convert signal that occurs before the dead time signal goes inactive will be vetoed.

4.7. *Dead Time*

The dead time signal that is passed to the digital section to be measured is the logical OR of three signals; the slow channel dead time, the fast channel dead time, and the preamp reset inhibit signal.

4.7.1. Fast Dead Time

The pile-up rejection window, F1, is used to measure fast dead time.

4.7.2. Slow Dead Time

Slow dead time is measured as the logical OR of the output of the slow discriminator, S1, and S2.

4.7.3. Preamp Reset Inhibit

The preamp reset inhibit disables events that occur during the preamp reset time. It can optionally be set (using jumpers on the DIB board) by the other segment reset or overthreshold event signals.

4.7.4. Dead Time Measurement

The system measures dead time with a digital counter counting at 1MHz (actually 2^{20}Hz), which is disabled when the dead time signal is active. This signal is read out into the telemetry in both the monitor rates (sampled at 1Hz), and in the events themselves (sampled at 2048Hz), as described in HSI_SYS_007.