THE RHESSI SPACECRAFT INSTRUMENT DATA PROCESSING UNIT

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Abstract. The Ramaty High-Energy Spectroscopic Imager (RHESSI) spacecraft is a NASA Small Explorer (SMEX) class mission. RHESSI is designed to image solar X-rays and gamma rays with high-energy resolution. The Instrument Data Processing Unit (IDPU) serves as the central RHESSI instrument on-board data-processing element. It controls and monitors the instrument operations, and provides a flexible telemetry collection and formatting system. The system responds autonomously to optimize science data collection over a wide dynamic range of conditions, handling up to 40 Mbps of telemetry during solar flares. This paper presents an overview of the IDPU hardware and software design.

1. Introduction

The Ramaty High-Energy Spectroscopic Imager (RHESSI) spacecraft is a NASA Small Explorer (SMEX) class mission. RHESSI is designed to image solar X-rays and gamma rays with high energy resolution (Lin *et al.*, 2002). The RHESSI Instrument Data Processing Unit (IDPU) serves as the central instrument data processing element for all RHESSI science package. It controls the instruments and collects and formats the instrument telemetry, and provides a single point interface between the spacecraft and instruments for commands, telemetry, and power. All instrument electronics not closely coupled to the instrument detectors reside in the IDPU.

The IDPU has significant performance challenges, while being significantly constrained by mass and power. State-of-the-art signal processing electronics is required for the germanium detectors to provide the throughput and resolution, but at a fraction of the power of previous systems. A variable data throughput rate up to 40 Mbits per second must be accommodated from the instruments to the spacecraft Solid State Recorder (SSR). The system must manage this throughput in an intelligent fashion to optimize the data return while not over-filling the SSR. The large quantity of aspect data collected must be reduced to a manageable volume by intelligent selection of critical subsets of the data to send. Active instrument control is required to maintain optimal instrument performance, such as spectrometer and imager thermal control, automatic detection of the excessive background generated when the spacecraft passes over the South Atlantic Anomaly (SAA) and

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appropriate response to limit data collection during that time, and sunlight/darkness detection and instrument re-configuration.

A key element to achieving high data throughput at low power is having the bulk of the data collection and formatting handled in field programmable gate arrays (FPGA) rather than in a microprocessor. This is similar to the FAST IDPU (Harvey *et al.*, 2001), allowing a modest microprocessor to provide the required intelligence while the routine tasks are carried out more efficiently in the FPGAs.

The IDPU is implemented in three physical boxes: the Instrument Power Controller (IPC), the Cryo Power Controller (CPC), and the VME chassis. The IPC contains the low and high voltage power converters for the instrument. The CPC is a power amplifier that generates the AC power required to run the cryocooler. The VME chassis contains the analog and digital signal processing elements. The VME chassis contains 12 6-U VME-sized cards, a backplane, and a small daughter card attached to the backplane. These cards include:

– A Data Controller Board (DCB) containing the central processor, spacecraft signal interfaces, backplane controller, and data formatter. The DCB also contains the analog and digital processing electronics for the particle detector.

– Nine Detector Interface Boards (DIB), which contain the analog and digital signal processing for each of the nine germanium detectors in the RHESSI spectrometer.

– An Aspect Data Processor (ADP) that processes the imager aspect sensor data from the Roll Aspect Sensor (RAS) and Sun Aspect Sensors (SAS).

– A Power Controller Board (PCB) which contains the various instrument power switching and controls, plus signal conditioning for the bulk of the instrument analog monitors such as currents, voltages, and temperatures.

The small daughter card attached to the backplane contains the interface to the second Roll Aspect Sensor, the RAS-PMT.

Figure 1 is a block diagram of the IDPU and how it connects to the rest of the instrument and spacecraft.

2. Spectrometer Data Flow

Signals from the germanium detectors in the spectrometer are processed by charge sensitive amplifiers attached to the spectrometer before being passed to the IDPU (Smith *et al.*, 2002). A total of 18 signals are generated, one for each segment of each detector (2 segments per detector). These signals are connected to the DIBs (2 segments are processed on each DIB board) where they are shaped, thresholded, and converted. The measured pulse height, corresponding to the energy deposited in the segment by the incident photon, is passed on to the detector interface field programmable gate array (DIF) on the DIB. The DIF combines the energy information with a time tag, segment identifier, and live time information to make a 32-bit event word per measured event. Event time provides microsecond accuracy,

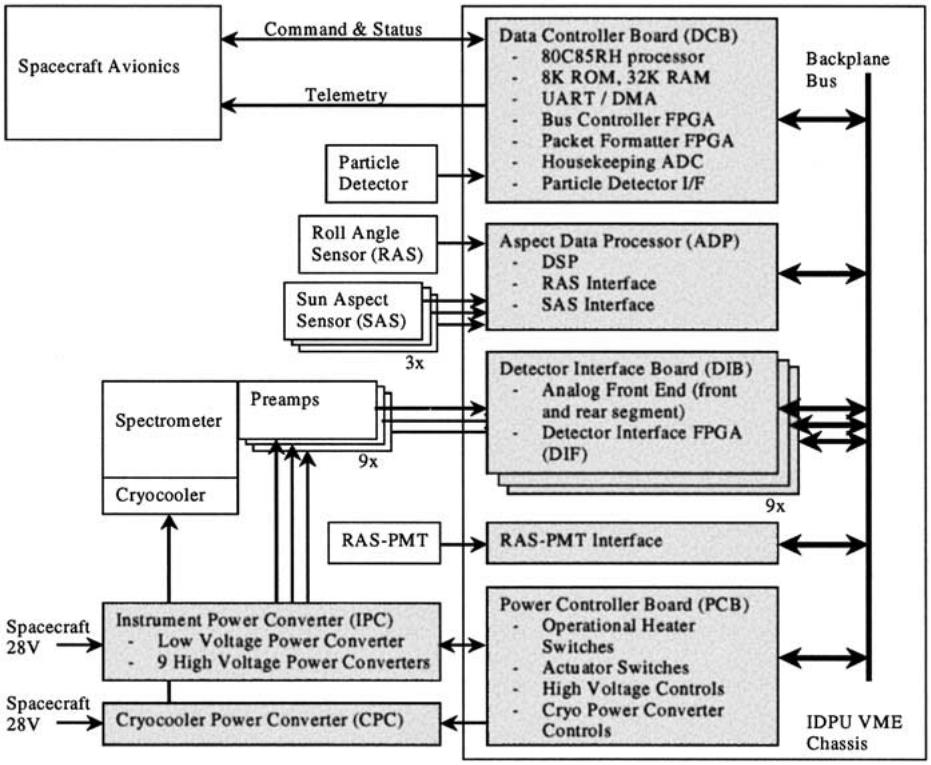

Figure 1. IDPU block diagram.

with millisecond dynamic range. These timing bits must be taken together with time tags events and the packet header time included in the event telemetry stream by the DCB to reconstruct the full event time.

Live time bits in each event provide information about the DIB throughput necessary to normalize the measured event rates. Live time is measured for each detector segment by a counter running at 1 MHz that is disabled when the DIB is not ready to process a new event because it is busy with the previous event. This live time counter is sampled at 2 KHz and read out in the live time field of the following 3 events (a few bits of the counter in each event). If events are happening so slowly that the DIB processes fewer than 3 events in the time between live time measurements, some of the live time bits are lost. This is acceptable, because at such low rates live time is relatively unimportant.

The DIF also incorporates monitor and fast rates counters, threshold DAC control, test pulser control, and DIB power control. Threshold DACs provide adjustable low-energy thresholding for events. The test pulser circuit generates a selectable rate of selectable amplitude pulses that are capacitively coupled to each detector. This provides a simple ground test for the electronics in the absence of photons, and also a calibration point for the processing electronics. The power

control provides the ability to power off the DIBs individually, and also provides over-current protection.

The DIF talks to the DCB over the backplane. The backplane consists of a 16-bit wide parallel data bus with addressing that allows the DCB to collect data or write control registers on each of the DIBs (or the ADP or PCB) on request. The backplane also accommodates one Event Transfer Request (ETR) signal from each DIB. This signal informs the DCB that the DIB has an event to be collected.

The DCB incorporates a microprocessor system plus a pair of field programmable gate arrays, the Bus Controller FPGA (BCF), and Packet Formatter FPGA (PFF). The FPGAs deal with the high throughput data under the direction of the processor, but without the processor having to deal with the data directly. This allows a very modest 8-bit processor to be used. The BCF arbitrates the backplane bus, collecting event data in response to ETR signals and rate data periodically. This data is passed on to the PFF, which then formats this data into CCSDS packets. Three types of packets are generated by the PFF:

– Event packets, consisting of a series of 32-bit events plus embedded time stamps.

– Monitor Rates packets, consisting of sets of monitor rate counter read-outs from the DIBs, each read out once a second.

– Fast Rates packets, consisting of readouts of the fast rates counters, read at rates of up to 16 kHz.

All packets include an automatically generated CCSDS packet header plus a science header containing key status information.

The PFF then passes completed packets on to the solid state recorder (SSR). The SSR is used in a FIFO mode, with data being continuously fed in by the IDPU, and read out during contacts to the transponder.

The BCF also allows the processor access to the backplane so that the processor can set instrument control registers and read back status registers from the DIBs and other boards.

3. Imager Aspect Sensor Data Flow

The imager includes a Roll Aspect Sensor (RAS) and three Sun Aspect Sensors (SAS) (Zehnder *et al.*, 2002). These sensors are optical instruments used to accurately determine the orientation of RHESSI with respect to the Sun. The data from these sensors is passed to the Aspect Data Processor (ADP) in the IDPU. The data is there processed using a DSP to greatly reduce the data rate to just that information that is required. The ADP then formats the data into CCSDS packets.

The BCF collects Imager Aspect data packets from the ADP on request (using another ETR signal). As ADP data is pre-formatted into packets, the BCF and PFF just pass them on without further processing. The processor can access ADP

registers to collect status information and load control information and software updates.

4. RAS-PMT Interface

A second Roll Aspect Sensor, the RAS-PMT, was added late in the development cycle to add redundancy to the original RAS (Hurford *et al.*, 2002). This new RAS requires a simple low-speed interface to the IDPU backplane. The circuit consists of a single RAS-PMT FPGA mounted to a daughter board attached to the backplane. The processor collects the data at a low rate (4 Hz), formats it into packets, and passes it to the spacecraft using the low speed state-of-heath interface rather than to the SSR. In addition to collecting data, the processor controls a static collection mode register and a DAC that sets the high voltage supply output voltage via the RAS-PMT FPGA.

5. Particle Detector

The particle detector is another relatively low-speed instrument used to monitor particle background and identify when the spacecraft is in the South Atlantic Anomaly (SAA). A charge sensitive amplifier is mounted together with the particle detector. The output of the amplifier is passed to the DCB, which contains shaping and two discriminators (one with a programmable threshold), followed by two counters included in the BCF. The BCF includes these particle detector rate counters in the Monitor Rates packets, sampled at 8 Hz. In addition, the processor reads these rates counters for use in the SAA detection software.

6. Spacecraft Data Interfaces

Spacecraft data interfaces to the IDPU include a high-speed (40 Mbps) interface to the SSR, a low-speed (9600 baud) RS232 interface to the spacecraft processor, and a stable clock interface. The SSR interface consists of an 8-bit data bus, a ready signal from the SSR, and a write strobe from the IDPU. Once ready, the SSR can ingest data continuously at 5 Mbytes per second with no handshaking required. The signals are conditioned with differential RS422 drivers/receivers.

The RS232 serial interface is used to exchange low-speed data between the IDPU and spacecraft, including:

– A housekeeping packet, containing IDPU state of health data.

– A diagnostic packet from the IDPU.

– Data from the Imager Aspect system, to be used as a possible backup to the Fine Sun Sensor by the Attitude Control System.

– Command packets from the spacecraft to the IDPU.

– Spacecraft status information, including instrument power, transponder, SSR, and ACS data, plus spacecraft time.

Data is exchanged once a second, following the 1Hz time tick. Diagnostic data is provided as required by the IDPU, with a fill packet sent if no diagnostic data is required. The spacecraft has a stable, oven-controlled oscillator that provides timing for all the spacecraft systems. This clock is provided to the IDPU in the form of a 1 MHz clock signal, a 1 Hz clock pulse (synchronous with the 1 MHz clock), and a time code provided over the RS232 interface once a second, corresponding to the time at the 1 Hz clock pulse. This time interface is used to synchronize and time tag all instrument and spacecraft data, providing relative timing accuracy to 1 μs, and absolute time accuracy to about 1 ms (after correlation of the spacecraft clock to UTC on the ground).

7. Processor

The processor provides control and monitoring of the instruments and data flow, collection of instrument housekeeping, and interaction with the spacecraft over the serial interface. The processing resources required for the IDPU are modest because the bulk of the high-speed data handling is done by FPGAs. The processor selected is an 80C85RH, an 8-bit radiation hardened processor with very low power requirements (< 100 mW). The processor runs at 3.3 MHz, and has an 8 kbyte PROM plus a 32 kbyte RAM. An 82C37RH DMA controller is used to facilitate data transfer between the IDPU and spacecraft over an RS232 serial interface contained in the BCF. The processor can access the backplane via the BCF as processor I/O registers. The BCF arbitrates processor access requests along with other use of the backplane.

An Analog to Digital Converter (ADC) on the DCB is used by the processor to collect analog housekeeping. The inputs to the ADC come via the backplane. Each board has an analog housekeeping multiplexer attached to a common analog housekeeping signal on the backplane, which is routed to the ADC. The IDPU controls this distributed multiplexer tree via registers on the boards controlled over the backplane.

8. Power Control Board

The Power Control Board (PCB) contains a number of ancillary functions for the IDPU, including:

– Operational heater power switching for the instruments (Grid tray heaters, RAS CCD heater, cold plate (anneal) heaters, imager grid tray heaters, spectrometer heater).

– Actuator power switches for the instrument actuators (spectrometer attenuators, vacuum valve, and RAS shutter).

– Cryocooler power and balancer waveform generators (58.6 Hz sine waves with separately programmable amplitudes and programmable relative phase).

– Detector high-voltage supply digital to analog converters, providing a control voltage to the detector high-voltage supplies on the IPC.

– Instrument voltage, current, temperature, and accelerometer monitors (via the DCB analog housekeeping system).

9. Software

The RHESSI IDPU flight software coordinates all instrument activities, as described in the processor section above. The software consists of a variety of tasks with moderate timing requirements; the high bandwidth tasks are performed by the FPGAs. The software is organized into 14 modules, totaling about 8000 lines of assembly code. The code is contained in a bipolar PROM, which is copied into RAM on boot-up. Code in RAM can easily be patched on-orbit as required by command load.

The IDPU software includes a very simple operating system for distributing processor time amongst tasks, handling interrupts, and handling hardware interfaces. Tasks are allocated time either as part of a foreground 'round-robin' polling loop, or at a fixed time slice as part of the 256 Hz timer-tick interrupt handler. The fixed time slice scheme allows deterministic timing and load leveling, while the foreground polling loop provides for non time-critical tasks which take too long to execute in an interrupt service routine. One additional interrupt associated with the DMA system allows that system to respond quickly to completed DMA transfers.

The software handles a number of routine tasks such as housekeeping data collection and formatting, command decoding and routing, instrument mode and power control, and thermal control. In addition, the software has a few tasks where it is required to take action on its own in response to data. A few of the more important tasks, at least in terms of understanding the RHESSI data set, are described below.

9.1. Attenuator control

The attenuators are used to extend the detector photon flux dynamic range. When the detector count rate is low, the attenuators are left open to maximize the detector sensitivity. As the count rate rises towards detector saturation first the thin and then, if count rates continue to increase, the thick attenuators are put in to cut down on the number of low energy photons that reach the detectors. The detector live times (from the monitor rates) are used to identify when the detectors are approaching saturation. Determining when to remove the attenuators is a little more difficult.

The amount of attenuation is a function of the photon spectra, which is information not available to the processor. This means that the processor cannot predict in advance what the rates will be when the attenuators are removed. Currently the software uses a fixed live time threshold to decide when to remove an attenuator, but this often results in the attenuator being put right back in. A time delay between motions is enforced to keep this from happening too often.

9.2. Decimation

The detector interface FPGAs have a decimation system for reducing electronically the number of low energy photons that are processed. This scheme causes a selectable fraction of the photons below a selectable energy level to be eliminated from the telemetry stream (they are still counted by the rate counters). This system does not keep the detector from becoming saturated, but does reduce the telemetry volume. The detector front segment decimators are used to reduce the data volume when the SSR starts to get full. Eight levels of increasing decimation are applied as the SSR fill level increases. When the SSR reaches 99% capacity, all events (front and rear segment) are eliminated as a last ditch effort to avoid over-filling the SSR while maintaining at least detector diagnostic data (rate counters).

Rear segment decimation is controlled from the ground. While rear segment flare count rates are rarely very high, they have a background rate that is a significant contributor to filling the SSR. The ground can select decimation of rear segment events at times of less interest, such as when the sun is not visible (behind the Earth), at the expense of non-solar science. Rear decimation can also be used in high latitude regions (as predicted on the ground) to limit background rates from penetrating particles.

9.3. South Atlantic Anomaly detection

The South Atlantic Anomaly (SAA) generates a high background level in the detectors from penetrating particles. To avoid filling the SSR with this background, it is desired to disable all detector events during these parts of the orbit. This can be done from the ground using a predicted envelope for this region, but the region moves around some. A conservative prediction results in good data being lost, while a less conservative prediction results in filling the SSR with background events. To improve the ability to determine when the spacecraft is in one of these regions, the software looks at the particle detector count rate. When the particle count rate is high, detector event rates are disabled. A conservative prediction of the SAA location is used on the ground to enable this feature when approaching the SAA.

10. Cryo Power Converter

The Cryo Power Converter (CPC) is a power amplifier that converts unregulated spacecraft 28 V to the AC power waveform required by the spectrometer cryocooler. A separately switched and current limited spacecraft 28 V service is provided to the CPC. The CPC actually has two amplifiers with independent waveforms: one for the cryocooler drive, and one for the active balancer used to minimize cryocooler vibrations. Waveforms for both amplifiers are provided by the Power Control Board. The CPC provides up to 100 W of power to the cryocooler at about 89% efficiency.

11. Instrument Power Converter

The Instrument Power Converter (IPC) takes unregulated spacecraft 28V power and generates the secondary voltages used by the IDPU and instruments. Three separately switched and current limited spacecraft power services are provided; one for the normal instrument operating power, and one for switched loads such as operational heaters and actuators, and a third for survival heaters. Survival heater power is routed to the instrument survival heater/thermostat circuits without conditioning. Switched power goes to the Power Control Board where FET switches control its distribution. In addition a 10 V supply powered by the switched power service provides power for the actuators. Actuator power is also routed to the Power Control Board where FET switches control its distribution.

The normal power bus is regulated and converted into a number of secondary voltages, including +5 V digital, ± 5 V analog, ± 12 V analog, +15 V, +28 V, and +100 V, with about 75% efficiency. Most of the secondaries are provided with about 0.5 V over-voltage so that they can run low-drop-out regulator/current limiters downstream on the boards. This provides clean power on the boards to reduce cross-talk, and also provides power isolation to isolate a failure on a board.

The regulated +28 V is used to power the detector high voltage supplies, also part of the IPC. These supplies provide a programmable output (controlled by voltages provided by the Power Control Board), up to 5000 V to bias the detectors in the spectrometer. Another 100 V programmable power supply is used to bias the particle detector (again using a control voltage provided by the Power Control Board).

The 100 V output of the IPC is used to supply the special Zener diodes used to heat the spectrometer cold plate for anneal cycles (and also to perform controlled detector warm-ups on the ground). The 100 V supply is routed via the Power Control Board, where it is switched and limited to provide a fixed current to the heater diodes.

12. On-Orbit Results

The RHESSI mission was launched in February 2002, and has had no problem meeting all its requirements to date. The IDPU continues to function flawlessly, providing data reliably with sufficient flexibility to accommodate all conditions encountered.

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