PFF Description and Functional Specification

Revision B
29 February 2000

HSI_IDPU_015D

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References.

HESSI IDPU ICD, D.W. Curtis, Version H, 19-Jun-1999

HESSI IDPU Packet Formatter FPGA Specification, D.W. Curtis, 98-Jun-12

HESSI IDPU Processor Specification, D.W. Curtis, 98-Jul-2

HESSI IDPU Telemetry Formats, Version D, D.W. Curtis, 1998-November-24

HESSI IDPU Detector Interface FPGA Specification, D.W. Curtis, 98-3-31

BCF Description and Functional Specification, D. Gordon, Rev. B, 29 February 2000

Revision History

Revision Number	Date	Change Summary
0.1	August 17, 1998	Initial Draft
0.2	April 23, 1999	Updates, Enhancements and Corrections
A	August 18, 1999	Formal Release - Corresponds to PFF Rev. 4
B	February 29, 2000	Documentation Update - reflects extended BCF bus timing

Introduction

The PFF (Packet Formatter FPGA) is a component of the Data Controller Board of the HESSI IDPU. Housed in an Actel the Actel 14100A (10K gates), it takes in data from the Bus Controller FPGA (via a 5 MHz 16-bit bus) which it formats into packets. The packets are then forwarded to the Spacecraft (S/C) via an 8-bit 5 MHz telemetry bus.

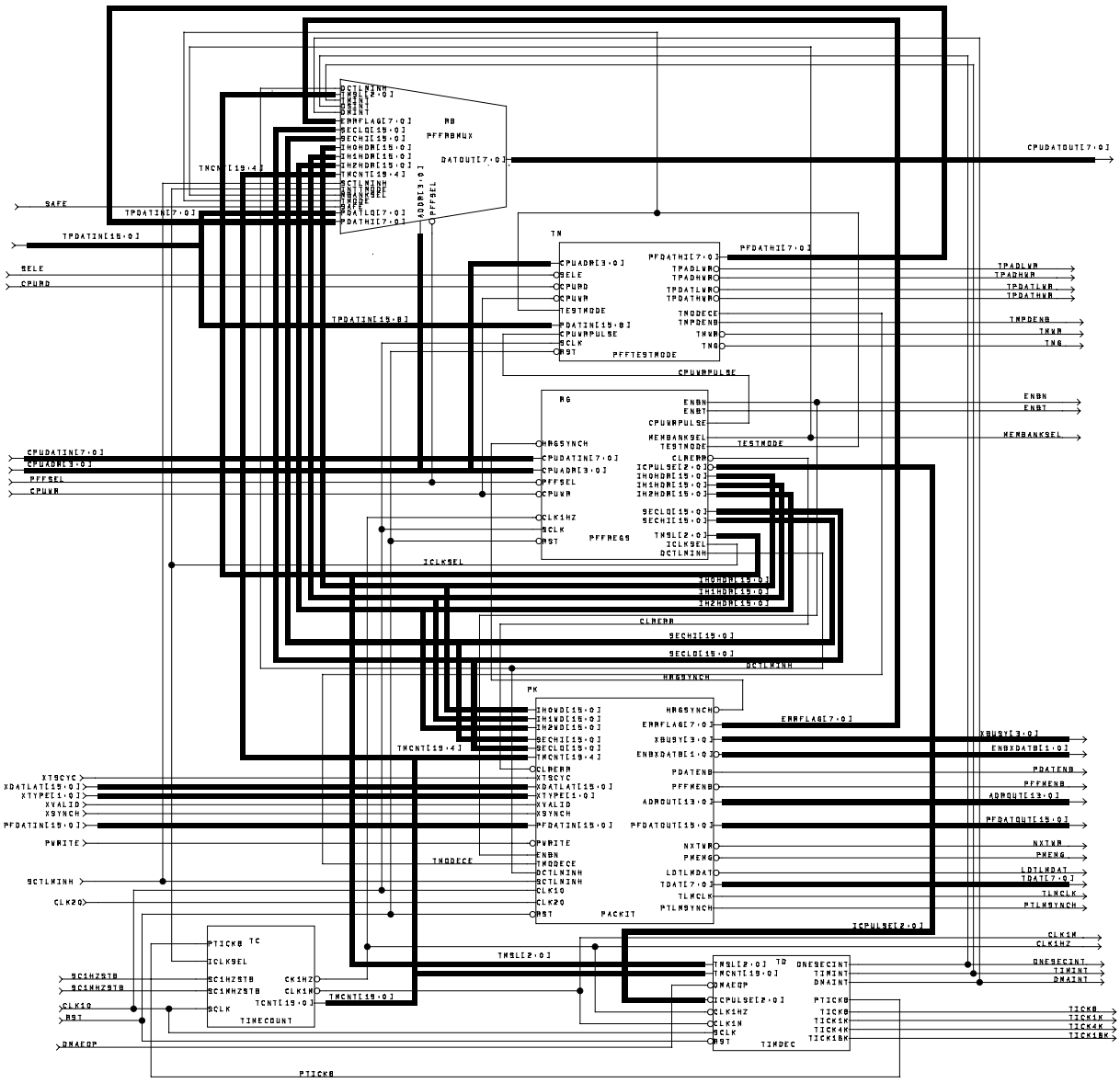

FIGURE 1. PFF - Overall Block Diagram

Figure 1 is a top level block diagram of the PFF. PACKIT, a module appearing in the lower center of the diagram, houses the fundamental PFF control logic. Driven by the BCF “X” bus (XDATA, XTYPE, XVALID,XSYNCH and XTSCYC), PACKIT collects data in 16-bit units, and transmits it to the spacecraft in packet sized units. The other modules form the PFF support system and programming I/F. Each subsystem is described below:

1.0 Central Timing Control

The 10 MHz master clock (referred to as SCLK or CLK10) is generated by the PFF from a 20 MHz master oscillator (CLK20). SCLK, forwarded to the BCF and to the DIF as BUSCLK, is used to generate the IDPU bus timing. CLK20 is used only by the PFF.

The Central Timing Control (TCOUNT) module appears on the lower-left side of the PFF. The PFF receives two S/C timing signals (a 1 MHz clock and a 1 Second timing pulse) and generates two strobes: CLK1M and CK1HZ, shown below. The strobes are forwarded to the BCF and the IDPU backplane (driving 9 DIF boards).

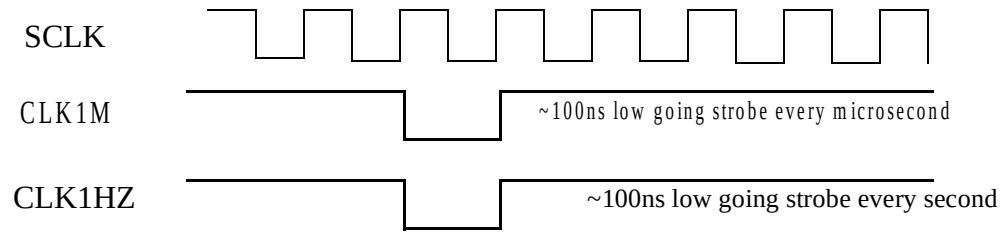

FIGURE 2. Clock and Timing Strobe Inputs

TCOUNT uses a synchronous 20-bit counter which is reset by the 1 second tick (CK1HZ) and clocked by the 1 MHz clock (CLK1M). The real-time count is passed onto the Packet Formatter subsystem (PACKIT) where it is used to timestamp telemetry packets as they are written into PFF memory.

The seconds register (or counter), a 32-bit synchronous, loadable counter, is housed in the PFFREGS module. It is clocked by CLK1HZ, and loaded by the CPU via the register interface. The seconds counter is not initialized by reset and will therefore retain its value during a “warm” reset (watchdog or commanded).

The PFF also generates timing strobes required by the BCF for Fast Rate and Monitor Rate read-out control. These (active high) pulses are: TICK16K (16KHz), TICK4K (4KHz), TICK1K (1KHz) and TICK8 (8Hz).

1.1 Internal Timer Option

There is an option to replace the spacecraft timing signals with internal clocks, which are generated by a divide circuit resident in the PFF. The internal clock option is selected by writing a 1 to bit 7 of the PFF Control Register (at address C0 hex).

When Internal Timer operation is selected, there will be a slight difference in frequency since all the clocks and strobes are derived from the 10MHz SYSCLK, rather than the spacecraft generated strobes. (S/C CLK1MHZ is actually 1,048,576 Hz. See the IDPU ICD for more details.)

2.0 PFF Registers and Readback Mux

The PFF registers are latched in response to CPU (driven by the 8085) bus writes. The programmable control and header information is described in Section 2.1 below.

To assure that telemetry header information is stable when written into PFF memory, the PFFREGS module generates a 100ns synchronized write pulse, derived from the longer CPUWR, an 8085 strobe. Thus the PFF register write pulse occurs “out of phase” with respect to the transfer of the header word into PFF memory.

The BCF preprocesses the upper 4 bits of the CPU address, and forwards two select lines to the PFF: PFFSEL and SELE. PFFSEL (address C) is used for general PFF functions. The upper half of SELE (address E) is used for PFF Testmode (see description below). The PFF readback mux merely steers data based on the CPU address and select lines.

2.1 Bus Registers

The PFF contains the following registers, mapped into 8085 IO address space as follows:

Address	Read Register	Write Register
C0	Control Readback Directly reads back Control Register	Control Register Bit 0: PF Memory Test mode setting this bit to one allows the processor to read and write the 32K x 16 Packet Formatter Memory. Bit 1: PF Memory Bank Select sets the upper bit (ADR14) of the PFF memory address. Bit 2: Telemetry Inhibit setting this bit halts the telemetry readout and causes a general reset of the packet readout subsystem (packet writing continues until memory fills). Bit 3: unused Bit 6-4: Internal Timer Interrupt Select Field Value -> Timer Frequency 0 - 8 Hz 1 - 16 Hz 2 - 32 Hz 3 - 64 Hz 4 - 128 Hz 5 - 256 Hz 6 - 512 Hz 7 - 1024 Hz Bit 7: Internal Timer Mode setting this bit causes the PFF to use internally generated clocks rather than the S/C inputs (1MHz and 1Hz). All Control Register bits are cleared to zero by reset.
C1	Status Readback Bit 0: Timer Interrupt (latched) Bit 1: One Second Interrupt (latched) Bit 2: DMA - EOP Interrupt (latched) Bit 5-3: Spares Bit 6: S/C Telemetry Inhibit (input RRECRDYF from the high speed telemetry I/F) Bit 7: SAFE - S/C status input	Pulses Bit 0: Clear Timer Interrupt Bit 1: Clear One Second Interrupt Bit 2: Clear DMA-EOP Interrupt Bit 7: Clear Error Flags clears all Packet Collection related Error Flags, which are readable at address C2

Address	Read Register	Write Register
C2	Packet Collection Error Status Readback Bit 0: Event Memory Full Error Bit 1: Event Long Packet Error Bit 2: Fast Rate Memory Full Error Bit 3: Fast Rate Long Packet Error Bit 4: Monitor Rate Memory Full Error Bit 5: Monitor Rate Long Packet Error Bit 6: ADP Short Packet Error Bit 7: ADP Long Packet Error	Not used
C3	Spare	Not used
C4	Seconds Register Low word: Bits[7:0]	Seconds Register Low word: Bits[7:0]
C5	Seconds Register Low word: Bits[15:8]	Seconds Register Low word: Bits[15:8]
C6	Seconds Register High word: Bits[7:0]	Seconds Register High word: Bits[7:0]
C7	Seconds Register High word: Bits[15:8]	Seconds Register High word: Bits[15:8]
C8	Instrument Header Register 1	Instrument Header Register 1: Bits[7:0] first byte shifted out as telemetry header
C9	Instrument Header Register 2	Instrument Header Register 2: Bits[7:0] 2nd byte shifted out as telemetry header
CA	Instrument Header Register 3	Instrument Header Register 3: Bits[7:0] 3rd byte shifted out as telemetry header
CB	Instrument Header Register 4	Instrument Header Register 4: Bits[7:0] 4th byte shifted out as telemetry header
CC	Instrument Header Register 5	Instrument Header Register 5: Bits[7:0] 5th byte shifted out as telemetry header
CD	Instrument Header Register 6	Instrument Header Register 6: Bits[7:0] 6th byte shifted out as telemetry header
CE	Subseconds Counter Bits[11:4]	not used
CF	Subseconds Counter Bits[19:12]	not used
E8	E8 through EB read back the PFF low data byte pointed to by the PFF Address Register. During this read cycle the upper data byte is latched into a register which can be read back at addresses EC-EF (see below).	Test Mode Data Register Low Byte
E9		Test Mode Data Register High Byte
EA		Test Mode Lower Address Register (maps to PFF Memory Address 7:0
EB		Test Mode Upper Address Register (data bits 5:0 map to PFF Memory Address 13:8) The PFF control register drives address bit 14.
EC	Upper data byte of PFF memory, previously latched by read of E8-EC (see above).	spare
ED		Create Write strobe to PFF memory. Data in Test Mode data registers is written into the PFF memory address pointed to by the PFF Test Mode address registers.
EE		
EF		

TABLE 1. PFF Internal Register Memory Map

Refer to the specific subsystems' description for further detail regarding the packet formatting status bits.

3.0 CPU Interrupts

The PFF latches and forwards three interrupts to the 8085. Interrupts are:

Interrupt Type	Signal Name	8085 Interrupt Input
One Second Interrupt	ONESECINT	RST 5.5
Timer Interrupt	TIMINT	RST 6.5
DMA Interrupt	DMAINT	RST 7.5

ONESECINT is caused by CLK1HZ (or its internally generated equivalent when the PFF is programmed for internal timer mode). The timer interrupt frequency is programmable via the PFF Control Register (Addr C0 hex, bits 6:4) as follows:

Timer Select Field	Timing Tick Interval
0	8 Hz
1	16 Hz
2	32 Hz
3	64 Hz
4	128 Hz
5	256 Hz
6	512 Hz
7	1024 Hz

Timing interrupts are not generated coincidentally with ONESECINTs. For example, if the Timer Select Field is programmed to 0, selecting 8 Hz, there will be 7 timer interrupts per second, plus the one-second interrupt.

The timing tick interval defaults to 8 Hz at reset.

DMA interrupt is caused by a falling edge on the DMA EOP signal driven by the 82C37.

All interrupts are latched and available as status via the PFF Status Register. They can be cleared via the PFF Pulse Register (see Section 2.1, "Bus Registers," on page 5).

4.0 PFF Memory

The PFF has direct control over all accesses to its private memory (a 32K x 16 bit SRAM) which is used for building packets. Normally the packet formatter system cycles through the memory at 10 MHz, performing 4 (potential) cycles continuously: a packet word write, a header word write, a packet word write and a S/C read. Cycle slots are only used when requested by the various subsystems: the BCF requests packet word writes; the PFF based header control and packet reader subsystems request header word write and S/C read slots. The timing of these cycles is described in further detail below.

The PFF generates a PFF Memory Chip Enable, which is asserted when the PFF anticipates a potential packet word write into PFF memory (as a result of an XBUS transfer) or continuously during packet readout. Chip enable is also asserted continuously during PFF Test Mode (described below).

4.1 PFF Test Mode

An alternate port has been provided to the PFF memory in order to facilitate diagnostics. This mode, which uses alternate drivers within the PFF, can be set by writing to the PFF Control Register bit TESTMODE. When TESTMODE=1 all the usual PFF memory drivers are tri-stated, and the TESTMODE drivers are enabled. The testmode data and address registers are writable at addresses E8hex to EBhex.

Writing to address EDhex creates a write strobe if TESTMODE is enabled, transferring the data in the data registers into the memory location indexed by the address registers.

Reading back can be accomplished by setting up the address register, reading from address E8hex for the lower data byte, and then reading from address EChex for the upper data byte. (NOTE: the lower data byte must be readout first, as this cycle performs the latching of the upper address byte.)

5.0 Packet Controller Subsystem

The subsystem PACKIT receives data from the BCF, which is in general transferred directly from the IDPU bus. The data is written into PFF memory during the available cycle slots for packet transfer. Header writing and packet readout occur in between the writing of packet words. A block diagram of PACKIT appears below:

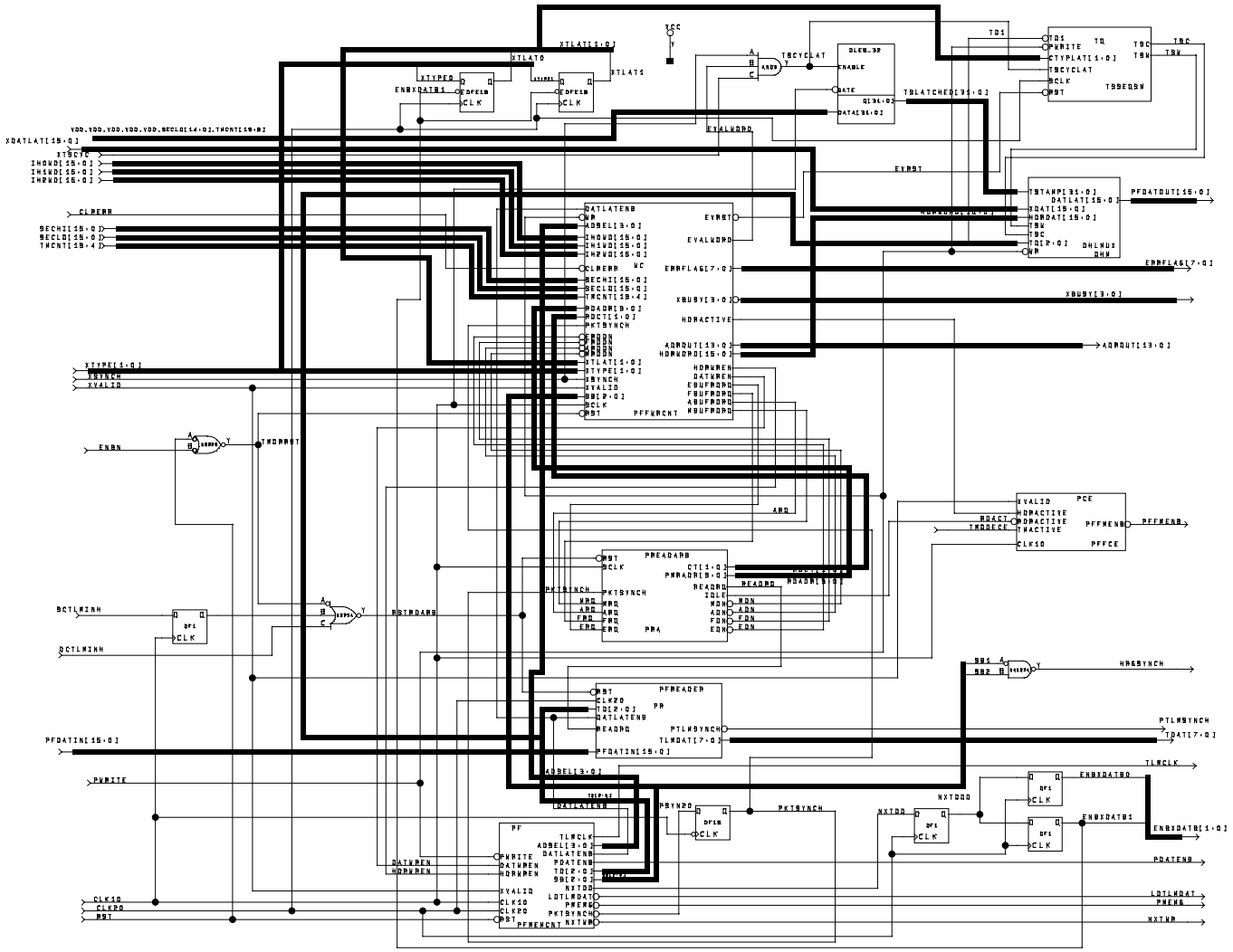

FIGURE 3. PACKIT Subsystem

5.1 XBUS Description

The BCF transmits IDPU data to the PFF via the XBUS, described below:

XVALID	strobe indicating a valid IDPU to PFF data transfer
XDATA[15:0]	16 bits of data being transferred
XSYNCH	start of data unit (cycle for rates, packet for ADP, event word for DIFs)
XTYPE[1:0]	type of data being transferred
XTSCYC	asserted during timestamp events

XTYPE is broken down as follows:

CYCLE TYPE	XTYPE CODE
DIF Event Cycle	0
Fast Rate Cycle	1
Monitor Rate Cycle	2
ADP Cycle	3

TABLE 2. Packet Formatter Cycle Types

The PFF, in return, generates XBUSY[3:0]. The XBUSY (active low) signals inform the BCF when packet memory is fully allocated, separately for each subsystem. (XBUSY signal indices map directly to the XTYPE codes.)

5.2 Spacecraft (High-Speed Telemetry) Interface

The PFF telemetry bus, consisting of 8 data bits, one synch signal (active low) and a 5 MHz telemetry clock, is designed to comply with the HESSI IDPU ICD. The PFF generates HRECCLK, the 5MHz telemetry clock which is forwarded to the S/C SSR (solid state recorder). Data and synch are transitioned on the rising edge of HRECCLK; the SSR clocks data in on the falling edge.

The S/C provides an asynchronous “TLMREADY” signal, whose deassertion is used to shut-down the PFF packet reader. A TLMREADY deassertion resets the PFF telemetry subsystem. Packet writing continues, but packet readout is halted. When readout recommences, pending packets are telemetered from the beginning of the packet queue. As PFF memory empties, the XBUSY signals are deasserted and IDPU data collection restarts. It is expected that during normal operation the TLMREADY signal will always be asserted.

High-Speed Telemetry can also be halted via the Telemetry Inhibit bit (Register 0xC0, bit 2) of the PFF Control Register. This processor controlled enable acts in exactly the same manner as the TLMREADY signal.

5.3 PACKIT operation

The “PACKIT” module, seen in Figure 3, is the heart of the PFF. It’s main subsystems include a memory timing controller, a packet write control subsystem, a packet reader and a high-speed telemetry multiplexer.

5.3.1 Memory Timing Control

The PFF memory timing is generated by PFMEMCNT, using CLK20 to cycle through an 8-state sequencer. Using two states for each memory cycle, PFF continuously outputs three write slots, and one memory read every 400 ns. The higher level PACKIT subsystems “plug into” PFMEMCNT.

A sample of the PFF memory timing is shown below:

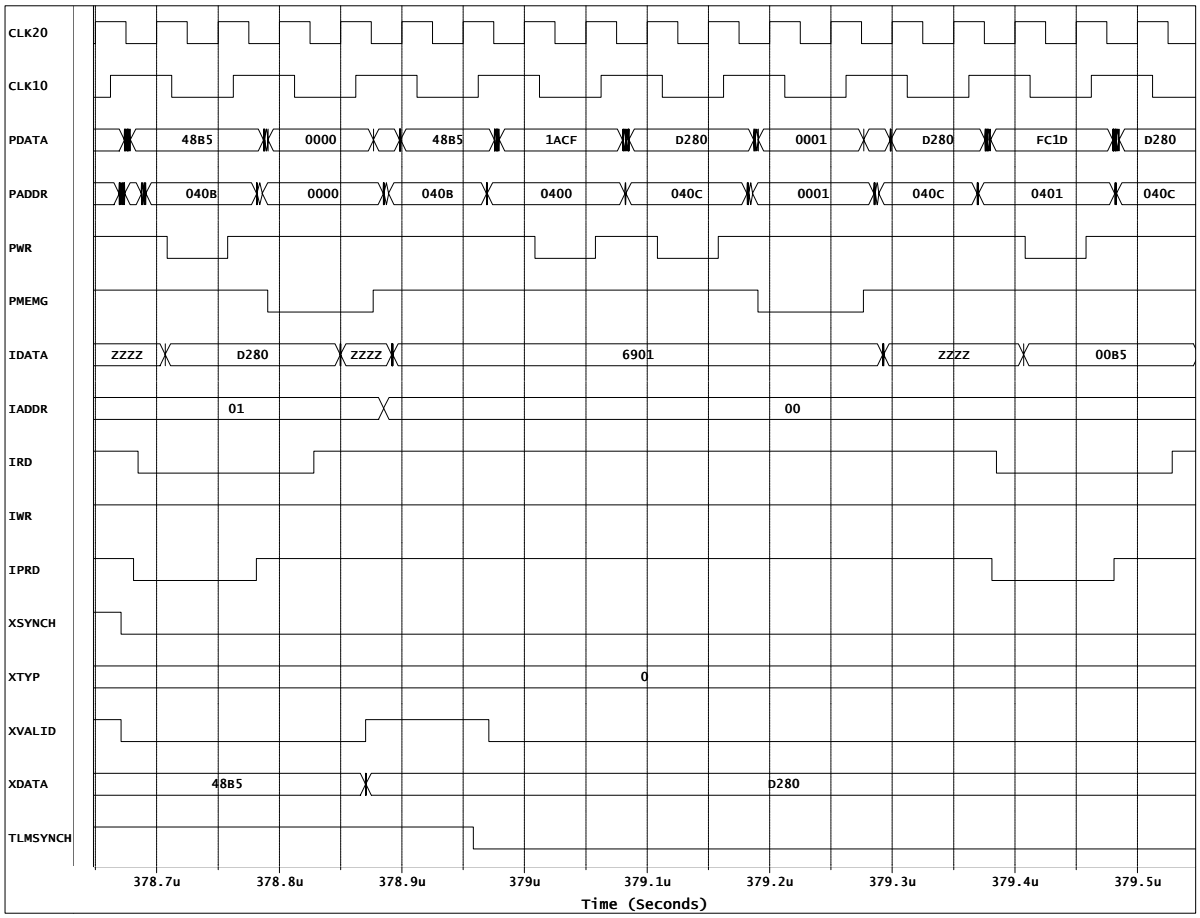

FIGURE 4. PFF Memory Timing

Figure 4 shows a few cycles of PFMEMCNT. Centered in the figure is a header write followed a packet word write. The packet reader subsystem has just been activated, as evidenced by the assertion of the TLMSYNCH signal. Packet readout occur when PMEMG strobes low. The IDPU reads and corresponding XBUS transfers are shown below the PFF memory signals.

5.3.2 Packet Writer

PFWRCNT sorts data coming in over the BCF I/F, steering each “type” to independent write controllers.

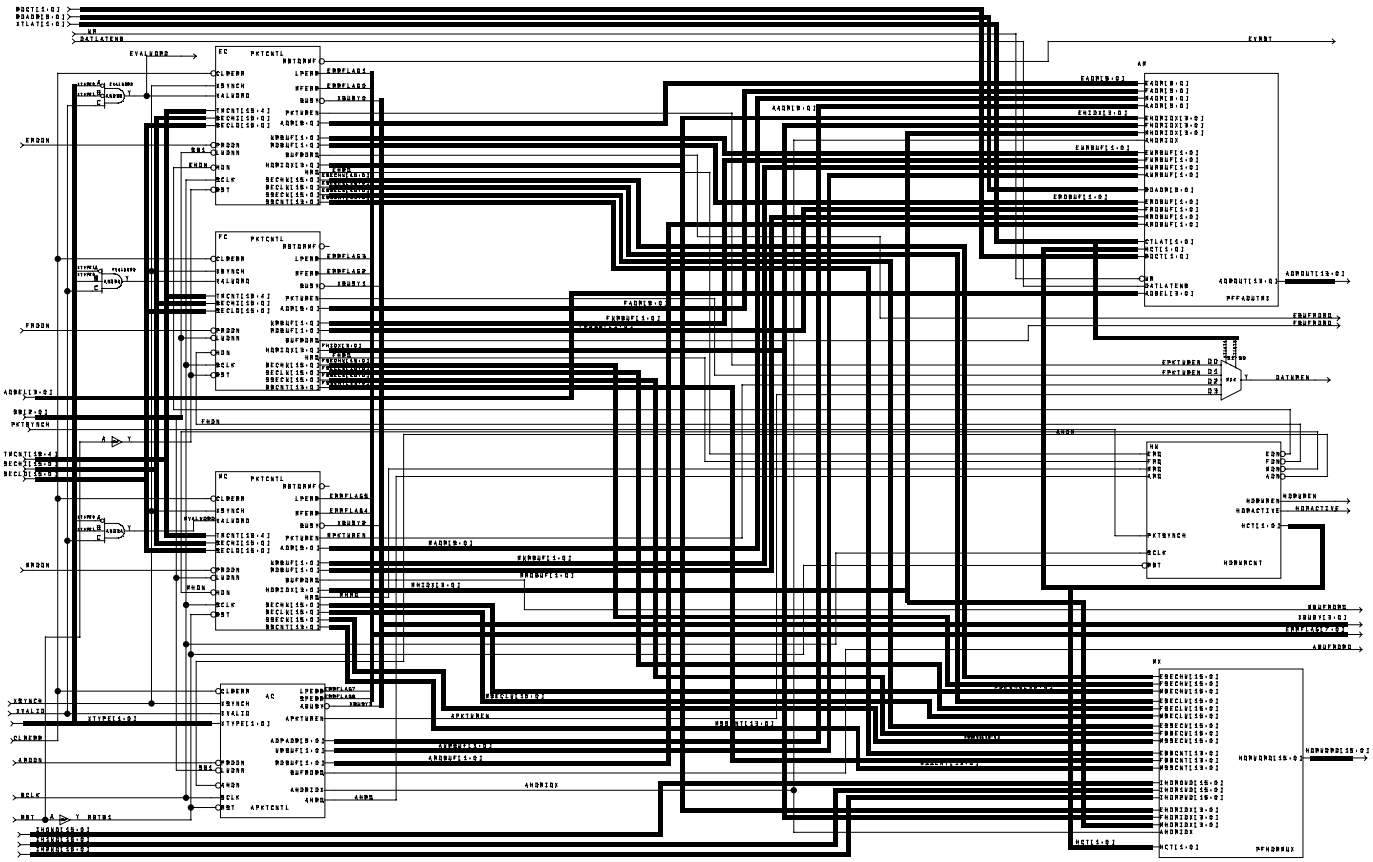

FIGURE 5. Packet Writer Subsystem

The four controllers are shown on the left side of Figure 5. The top three, servicing DIF events, Fast Rates and Monitor Rates, are internally identical. They are enabled only when the XTYPE relevant to their subsystem arrives with an XVALID strobe. The bottom left module, slightly different, services the ADP XBUS transfers.

Each controller operates by searching for a “start of packet” synch pulse. When a packet is started, a header request is queued, activating the header control module shown in the middle right of Figure 5. For the three systems requiring full header construction (the ADP inserts its own header information), packet data information is stored into PFF memory beginning at address: SEG ADDR + 000B HEX. The first 11 words of each packet, reserved for the header, are allocated as follows:

ADDR	WORD TYPE	WORD VALUE (in HEX)
0000	First Half of Synch Word	1ACF
0001	Second Half of Synch Word	FC1D
0002	Secondary Header - includes Application ID	0864 for DIF events 0865 for Fast Rates 0866 for Monitor Rates
0003	Source Sequence Count - 2 bit grouping flag ORed with the 14 bit source sequence count	C000 HEX OR SSCNT
0004	Packet Length (1091 decimal)	0443
0005	Seconds Counter - first two bytes	S[3:2]
0006	Seconds Counter - second two bytes	S[1:0]
0007	Subseconds Counter	SS[1:0]
0008	Instrument Header - first two bytes	I[5:4]
0009	Instrument Header - middle two bytes	I[3:2]
000A	Instrument Header - last two bytes	I[1:0]

TABLE 3. Header Word Definition

The ADP data writing starts at SEG ADDR + 0002 HEX and the header control writes only the Synch word at the beginning of each packet.

Subseconds and seconds information are latched individually by each of the three write control subsystems, as “start of packet” is detected. The header controller arbitrates between the sub-systems; the header multiplexer, shown at the bottom right of Figure 5, selects the data driven to PFF memory based on the selected system, and its current header address.

Separate source sequence counters are maintained by the three full-header write control sub-systems. This 14-bit counter, cleared by a RESET, increments each time a complete packet is written into PFF memory.

Each write control module outputs a write-enable after finding a synch, and holds the enable until detection of the end of packet. The subsystems’ enables are compared to XTYPE codes as they arrive with XVALID on the XBUS I/F, and used to gate the PFMEMCNT data write strobes.

The various subsystems are assigned PFF memory segments as follows:

Subsystem	PFF Memory Segment Address (HEX)
DIF Events	Buffer 0: 0000-0226 Buffer 1: 0400-0626 Buffer 2: 0800-0A26 Buffer 3: 0C00-0E26
Fast Rate Events	Buffer 0: 1000-1226 Buffer 1: 1400-1626 Buffer 2: 1800-1A26 Buffer 3: 1C00-1E26
Monitor Rate Events	Buffer 0: 2000-2226 Buffer 1: 2400-2626 Buffer 2: 2800-2A26 Buffer 3: 2C00-2E26
ADP Data	Buffer 0: 3000-3226 Buffer 1: 3400-0626 Buffer 2: 3800-3A26 Buffer 3: 3C00-3E26

TABLE 4. PFF Memory Subsystem Allocation

As can be seen, PFF memory address bits 12 and 13 determine the subsystem (with bits corresponding exactly to the XTYPE definitions), while PFF memory address bits 10 and 11 are the quadruple buffer index for each subsystem. There is one extra bit (PFF memory address 14) which can be used to select between the upper half and lower half of PFF memory. PFF ADDR14 defaults to zero and is settable via the PFF Control Register (see Table 1 on page 6), in case of a failure in the lower half of PFF memory space.

The PFF memory address mux appears in the top right of Figure 5. This purely combinatorial module pays attention to PFMEMCNT, and steers the appropriate READ, WRITE DATA, or WRITE HEADER address to the PFF memory address drivers.

Data muxing is done at the top level of the PACKIT subsystem (shown at the top right of Figure 3). The data mux is also where the time-stamp is inserted for any time-stamp events arriving on the X-Bus Interface. (See the IDPU ICD for a definition of timestamp events.)

Each write controller cycles through all of the four buffers continuously, and keeps track of buffer readout. For the DIF event, and Rates subsystems: and XBUSY is asserted on a per subsystem basis if a subsystem is writing to its last buffer, and the previous three buffers have not yet been serviced by the Packet Readout Control (see below). For the ADP, the XBUSY asserts if its memory is half full (two unread buffers in the queue). (When XBUSY[*n*] is asserted, the BCF stops reading IDPU data for subsystem *n*.)

5.3.3 Packet Readout Control

Figure 6 shows the PFREADARB module. It looks for read requests, arbitrates between the various subsystems, and reads out (whole) packets as they become available.

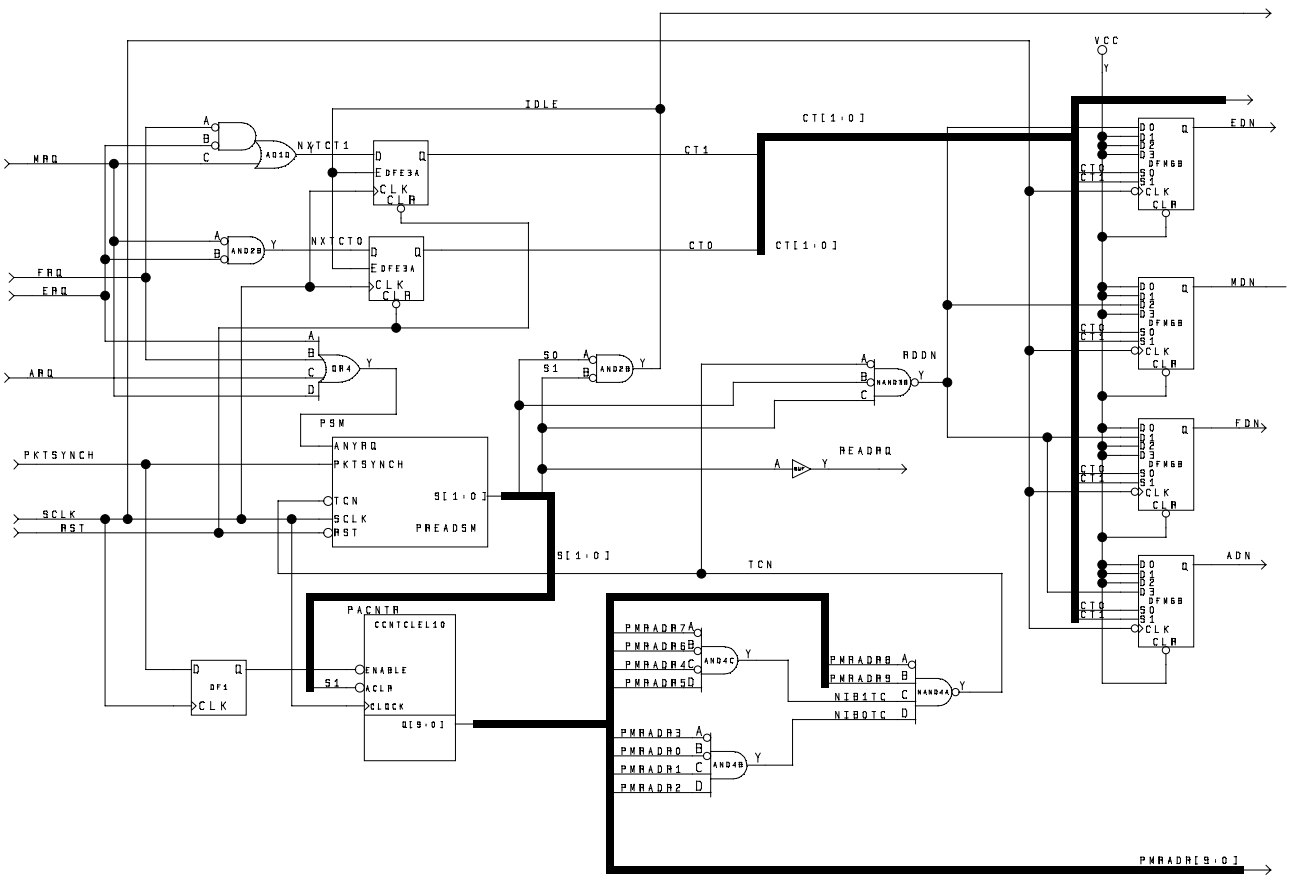

FIGURE 6. PFF Read Arbitor

After writing complete packets into PFF memory, each subsystems' write controller posts a READRQ to the PFF read arbitor. The subsystems are serviced according to the following fixed priority:

Priority	Subsystem
1	Monitor Rates
2	DIF Events
3	Fast Rates
4	ADP Packets

Once a subsystem's request is granted, the READARB module reads out a complete packet, forwarding the address to the PFF Memory Address Mux (described above). During any packet readout, the state machine activity is forwarded to the High-Speed Telemetry Mux (described below) where it causes the assertion of TLMSYNCH.

Due to a "recovery" cycle in each packet requestor's subsystem, upon termination of a packet, a lower priority subsystem can "steal" the next read-out slot. For example, if the ADP and DIF event subsystems are both constantly requesting read-slots (assuming no other subsystems are active), the read-out bandwidth will be split evenly between the two competing subsystems.

5.3.4 High-Speed Telemetry Mux

PFREADER drives the 8-bit telemetry data bus. It transfers a 16-bit word read out every 400ns via a 2 to 1 mux into two 8-bit units transmitted to the S/C every 200ns. Telemetry clock (200ns) is a derivative of PFMEMCNT, the master timing control for the PACKIT module. A timing diagram below shows the end of a high-speed telemetry packet, with corresponding PFF memory reads.

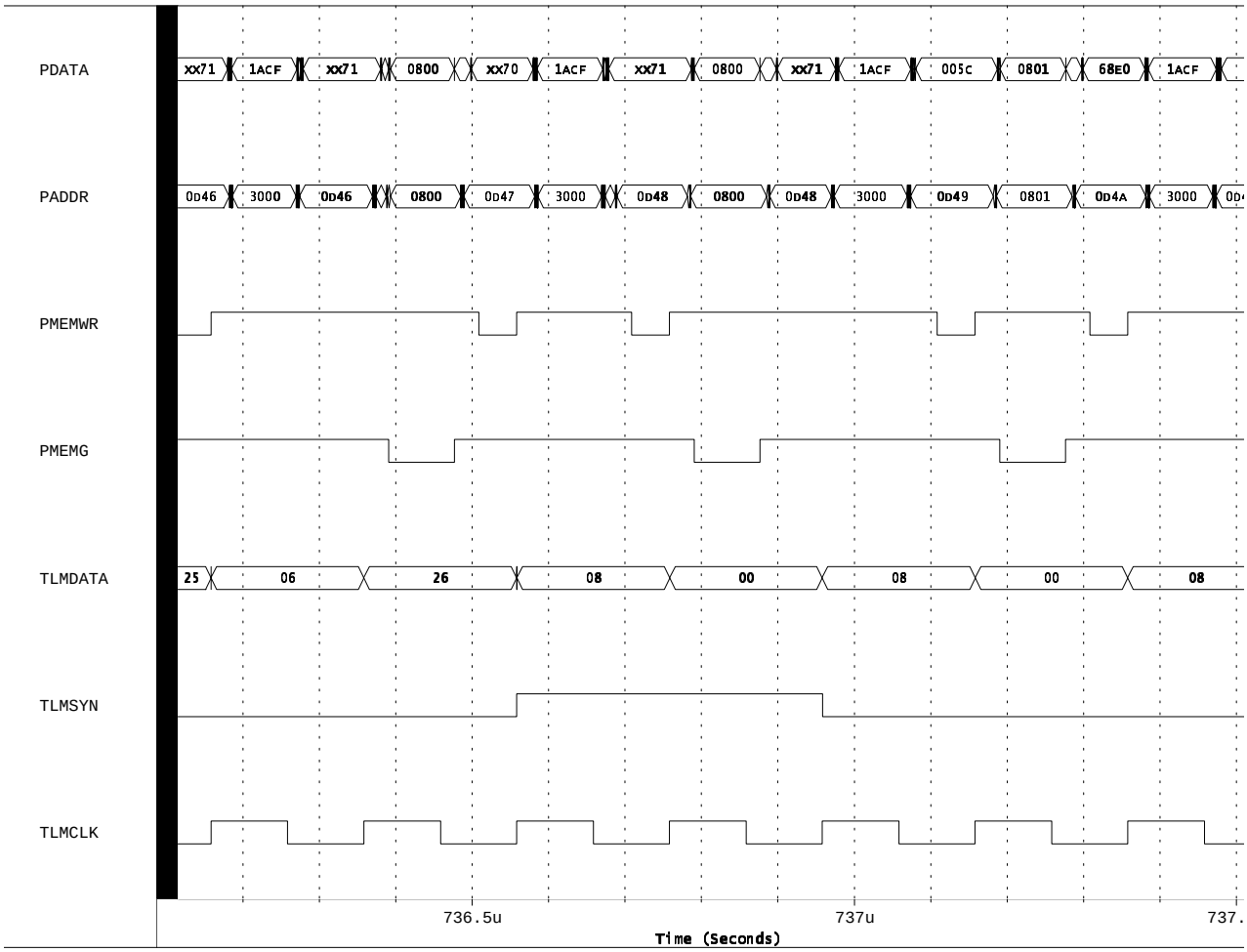

FIGURE 7. High Speed Telemetry Timing

Figure 7 is constructed from a simulation in which PFF memory is programmed to supply PFFMEMDATA = PFFMEMADDR, so the end of the packet (in this case an DIF event packet) shows up as data = “last packet word address” = 0626 HEX. It is followed by a readout of the next DIF event buffer, starting with data = “first packet word address” = 0800 HEX. (During actual operation this first packet word would always be 1ACF, the first half of the synch word.)

Figure 7 shows an instance where back-to-back DIF event readouts have been granted consecutive packet slots. In this case TLMSYN deasserts between packets for two TLMCLKs. When consecutive packet readout slots are granted to different subsystems (i.e. and ADP packet following a DIF Event packet), TLMSYN remains asserted (low).