DIF Description and Functional Specification

Revision C
29 February 2000

HSI_IDPU_010E

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References.

HESSI IDPU Backplane Signals, HSI_SYS_019F.doc, D.W. Curtis, 1999-Apr-13

HESSI IDPU Detector Interface FPGA Specification, D.W. Curtis, 98-3-31

HESSI Telemetry Formats, HSI_SYS_007C.doc, Version D, 1998-November-24

BCF Description and Functional Specification, D. Gordon, Rev. B, 29 February 2000

Revision History

Revision Number	Date	Change Summary
0.1 to 0.6	Apr. 1998 - Feb. 1999	For PreRelease Revision History see page 2
A	June 9, 1999	Formal Release - corresponds to DIF FPGA Rev. 3 Includes following modifications: AFEPOW is active low before it is routed to the output buffer Lists signals which are tristated when AFE Power is off. Assertion level (active high/low) of AFE inputs specified LiveTime Counter Freeze added Upper 12 bits of Event Energy are inverted by input latch Fast Rate Counter Recovery Time described
B	August 16, 1999	Corresponds to DIF FPGA Rev. 4 Includes following modifications: Input latch is moved to after the dither adder stage (modifies event hold time requirement). Event VETO function added
C	February 29, 2000	Documentation Update Only - (still at DIF FPGA Rev. 4) Timing updated to agree with BCF Rev. 8 - Extended IDPU Reads/Writes

PreRelease Revision History.

Revision Number	Date	Change Summary
0.1	April 22, 1998	Initial Draft
0.2	May 15, 1998	More detail and graphics; pulser programmable frequency added.
0.3	June 12, 1998	DAC Strobes (5) and DAC Data Register added; Individual (3) Power Switches added; IDPU bus width changed from 8 bits to 16 bits
0.4	September 22, 1998	Added AFE Power Shutdown Added ADC shutdown between conversions Modified DAC I/F (to accommodate quad threshold DAC). Changed all AFE inputs to active low Added 2 KHz livetime counters; deleted rejected events counters.
0.5	November 12, 1998	Added Test Mode Pulse Register - created Status Register - moved and expanded
0.6	February 19, 1999	Increased size of Rear Fast Channel Valid Monitor Rate Counter Swapped readback of high and low bytes of monitor rate counters Added terminal count “lock-in” for all monitor rate counters Corrected miscellaneous mistakes in the document

Introduction

The DIF is a collection of logic housed in an FPGA (the Actel 14100A, an ACT 3 device with 10K gates). One DIF is located on each of the nine event processing boards present in the HESSI IDPU. Each DIF consists of a bus interface and control unit, programmable registers, event processing modules for both front and rear detectors and various counters and timers. The main components appear in the block diagram shown below:

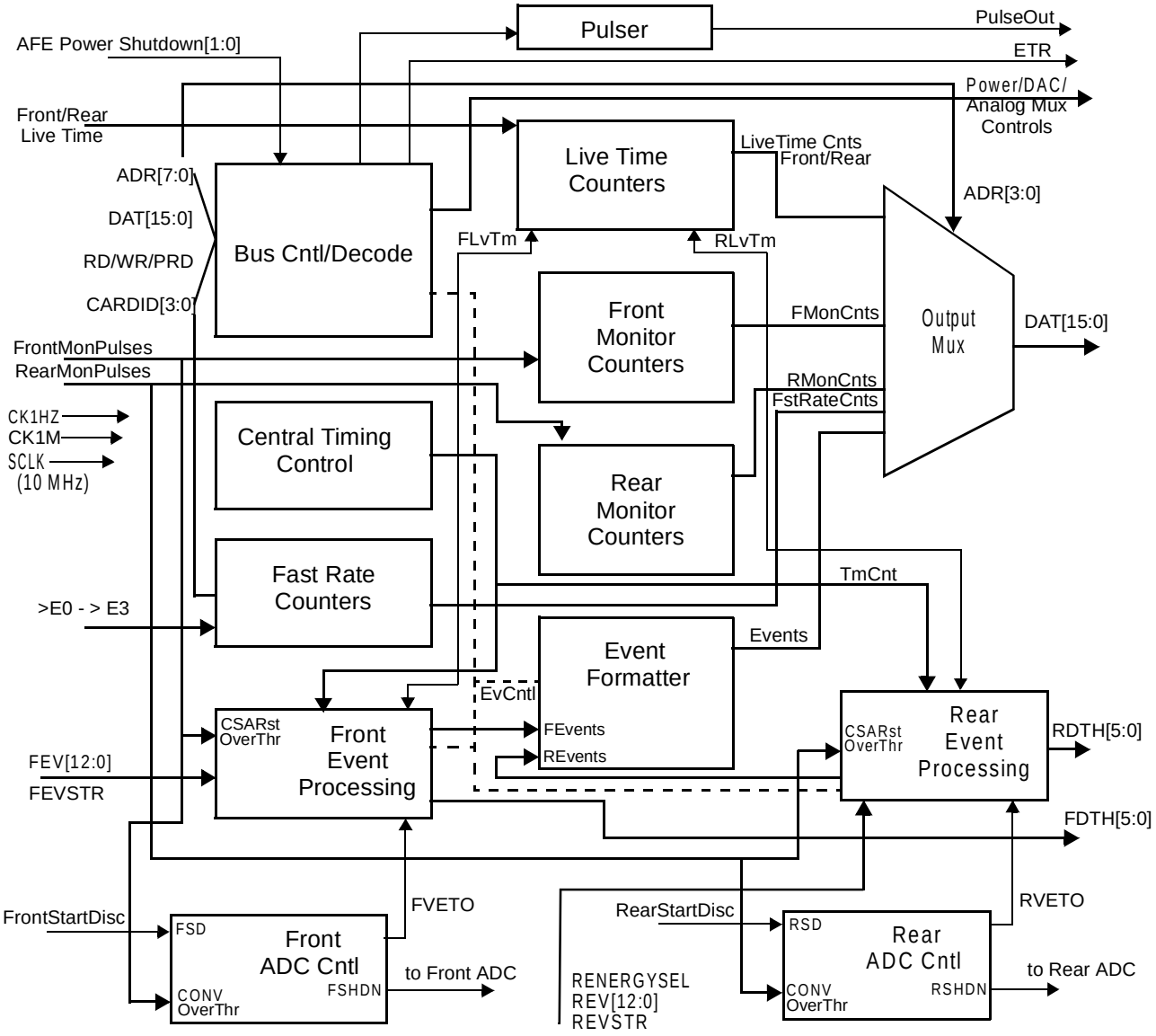

FIGURE 1. DIF - Overall Block Diagram

Components descriptions follow:

1.0 Bus Control/Decode

The DIF responds to read and write accesses from a master controller card. An encoded 4-bit CARD-ID uniquely identifies each event processing board. A read to a matching ID from the master processor enables the DIF or associated card data onto the IDPU backplane. A write from the master processor strobes data into the addressed DIF register. Additionally, each DIF can request action (event reads) from the master controller by asserting its ETR signal.

Bus timing is set by and synchronized to the 10 MHz system clock driven by the Data Controller Card. The bus control, data and address signals are described in the HESSI IDPU Backplane Signal Specification and the BCF Functional Description. The IDPU write cycle (performed exclusively by the 8085 resident on the Data Controler board) is pictured in the BCF Functional Description. IDPU hardware subsystem readouts are shown below, in Figure 2. PRD, asserted during a read cycle one-half of a clock cycle before RD occurs, is used to warn the count-latching state machines (see below) when a read is pending, so they can inhibit latch-loading. (See sections below describing Monitor and Fast Rate Counters.)

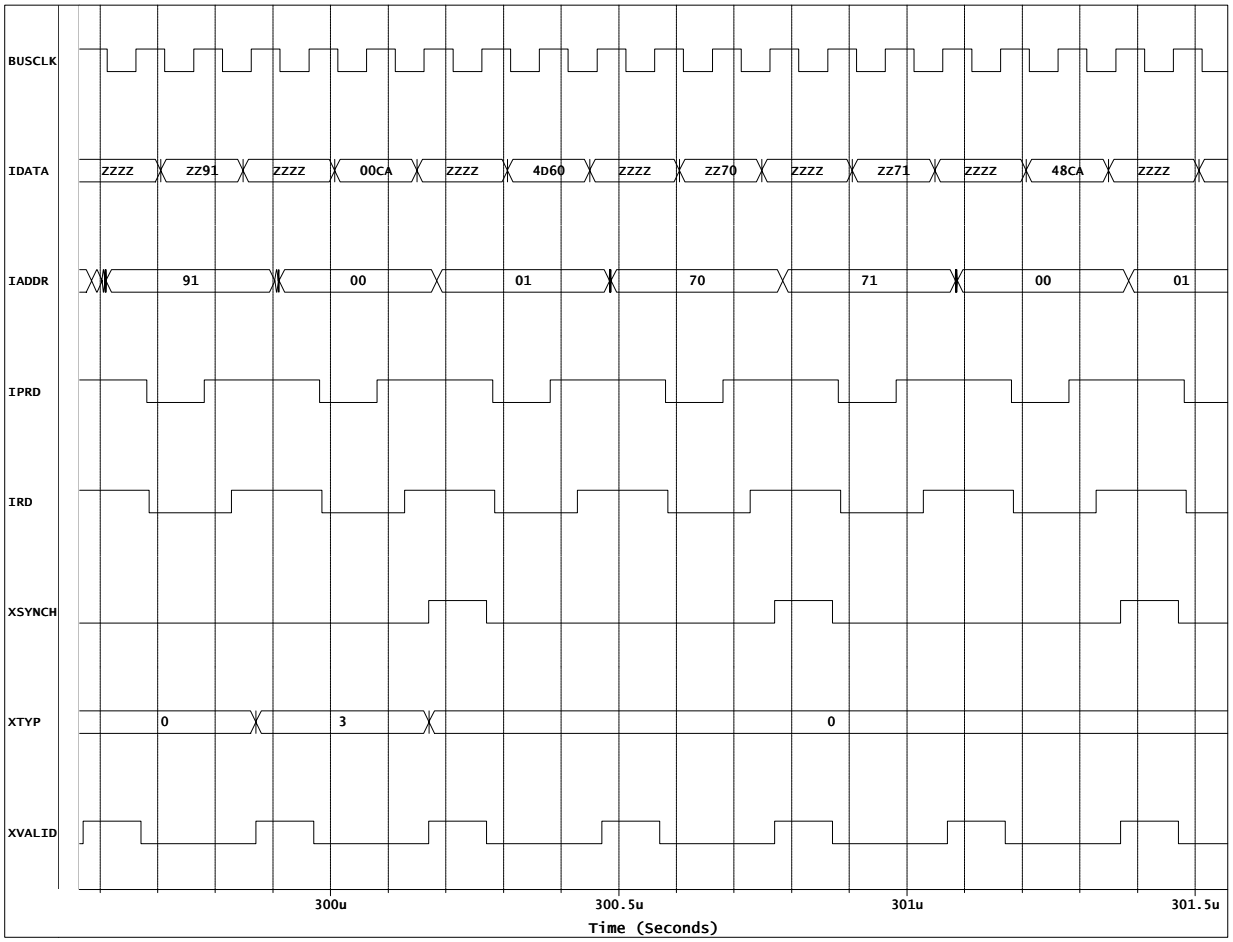

FIGURE 2. IDPU Read Cycles

An active low reset signal, also driven by the master controller card, serves to initialize all the DIFs.

1.1 Bus Registers

Each DIF contains the following registers (or external DACs):

Address	Read Register	Write Register
X0	Event Data - first 16 bits of a 32-bit event word (NOTE: Table 6 and Table 7 on page 16 detail the Event output word format.)	General Register/Controls Bit 0: Spare Register Output Bit 1: AFE Bit 2: TP (Test Pulser Power) Bit 3: Enable Overcurrent Shutdown Outputs are active high, with reset default to deas-serted (low).
X1	Event Data - second 16 bits of a 32-bit event word (NOTE: Table 6 and Table 7 on page 16 detail the Event output word format.)	Global Enables/Controls Bit 0: EventRequest Enb Bit 1: Pulser Enb Bits 3-2: Test Mode Control Field 00 => Normal (test mode disabled) 01=> 1 MHz Clock = Event Strobe 10=> 62.5 KHz Clock = Event Strobe 11=> Pulser Output = Event Strobe Bits 7-4: Test Mode Parameter Field sets test mode upper energy bits
X2	Fast Rate - first of formatted fast rate data words, latched every “collect-time” clock. (dependent on CARD-ID) (NOTE: Table 3 and Table 4 on page 12 detail the Fast Rate output word format.)	Front Detector Enables Bit 0: Event Enb Bit 1: CSA Reset Enb Bit 2: Over Threshold Enb Bit 3: Decimation Enb Bit 4: Decimate Any Bit 5: Dither Enb
X3	Fast Rate - second of formatted fast rate data words, latched every “collect-time” clock. NOTE: CARD-IDs 0,1 and 2 supply only 16-bits of fast rate counter data, available at address X2 only.	Front Decimation Parameters Bit 3-0: Decimation Count Bit 7-4: Decimation Energy
X4	BITS: 15-8: Front PreAmp Reset Count - a 16 bit counter, latched once/second and com-pressed to 8-bits for one byte read-out. BITS: 7-0: Front Slow Channel Valid Count - a 17-bit counter, latched once/second and com-pressed to 8-bits for one byte read-out.	Rear Detector Enables Bit 0: Event Enb Bit 1: CSA Reset Enb Bit 2: Over Threshold Enb Bit 3: Decimation Enb Bit 4: Decimate Any Bit 5: Dither Enb

Address	Read Register	Write Register
X5	BITS: 15-8: Front Slow Channel Over ULD Count - a 9-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Front Fast Channel Valid Events - a 19-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	Rear Decimation Parameters Bit 3-0: Decimation Count Bit 7-4: Decimation Energy
X6	BITS: 15-8: Front Live Time Count - the 8 MSBs of the 20-bit “live-time” counter. Latched once/second BITS: 7-0: Rear Preamp Reset Count - an 18-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	
X7	BITS: 15-8: Rear Slow Channel Valid Count - a 14-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Rear Slow Channel Over ULD Count - a 8-bit counter, latched once/second and compressed to 8-bits for one byte read-out.	Pulse Register Bit 0: Clear Latched Shutdown (Pulse)
X8	BITS: 15-8: Rear Fast Channel Valid Events - a 19-bit counter, latched once/second and compressed to 8-bits for one byte read-out. BITS: 7-0: Rear Live Time Count - the 8 MSBs of the 20-bit “live-time” counter	Pulser Frequency Select Bit 3-0: Select from 11 frequencies ranging from 1 Hz to 1KHz
X9-XB	Not used	Not used

Address	Read Register	Write Register
XC	DIF Status Bit 0: AFE Power Bit 1: Enable Overcurrent Shutdown Bit 2: Overcurrent Status - Latched over-current indicator, set by either of two inputs from the AFE, cleared by pulsing "Clear Latched Shutdown" (see Address X7). Bit 3: AFESHUTDOWN status line 0 Bit 4: AFESHUTDOWN status line 1 Bits 3 and 4 are the direct inputs from the AFE current monitoring circuitry. Bit 5: Test Pulser Power (bit 2 of the General Register/Controls - Addr X0) Bit 6: Front Event Enable (bit 0 of the Front Detector Enables Register - Addr X2) Bit 7: Rear Event Enable (bit 0 of the Rear Detector Enables Register - Addr X4) Bits 15:8 - a readback of the Global Enables/Controls Register, located at Address X1	DAC Programming Register Bit 11- Bit 0 programs the DAC data word. This word is latched following any DAC write cycle, holding the DAC data bus the last programmed value. Bits 14 - 12 control the 8408, a quad DAC used to drive the AFE threshold settings. Bit allocation: Bit 12: Creates Data Strobe 0 Bit 13: Creates Data Strobe 1 Bit 14: Drives SELA Bit 15: Creates Write strobe to Pulser DAC (an AD7545) Data and Write strobes (300ns) are generated by DIF sequential logic, based on the state of bits 12, 13 and 15, following any write to address XC. SELA is latched in the same manner as the DAC data word. All signals are passed onto the DACs without a change in polarity. NOTE: Data and write strobes are active low. For further information, see DAC specifications.
XD - XF	Not used	Not used
F0	Not used	Analog Mux Select Bits 7-4: CARD-ID Bit 3: Analog Mux Select (1 -> set AMUXENB1) (0 -> set AMUXENB0) Bits 2-0: Analog Mux Addr If data bits 7-4 match CARD-ID, the DIF generates an analog mux select.

where X= CARD-ID and F=> broadcast to all DIFs (write commands only)

NOTE: All register bits default to zero (=> inactive for enables) at reset. The Event Enables also serve as an reset line for the event processing modules. (Monitor and Fast Rate Counter modules are reset only by the general DIF reset line.)

1.1.1 Analog Mux Select

If a write to the address F0 occurs, each DIF looks at data bits 7-4. If this nibble matches the CARD-ID, the DIF latches an assertion of an analog mux enable (AMUXENB[1:0] (active high), which enables one of the board's analog muxes onto shared wire resident on the IDPU backplane. During this bus cycle, the lower data bus nibble is decoded and latched to generate a two-bit enable and three bit mux channel address. AMUXENB will be asserted only for the CARD with the matching ID in the upper data nibble; the 3-bit channel select, however, will update for each board with any write to address F0.

1.2 Bus Control

The bus control unit handles the event request and Front/Rear detector arbitration. Each event processing module requests service upon reception of an event. This includes AFE event strobes, CSA reset events and OverThreshold events. There are thus six unique types of events which may request service; they are handled using the following fixed priority ordering:

Rear Detector Events
Front Detector Events
Rear CSA Reset Events
Front CSA Reset Events
Rear OverThreshold Events
Front OverThreshold Events

The bus controller asserts ETR to the Master Controller card via the IDPU backplane once it has determined that a detector requires servicing. It then looks for reads to its CARD-ID at address X0 or address X1. Upon detection of a read to the second event word address (X1), the controller sends a "DONE" signal to the selected event processing module.

2.0 Central Timing Control

Central timing control receives clocks from the Controller card via the IDPU backplane. The master clock (SCLK) for the DIF is a 10 MHz system clock. The 1 MHz (CLK1M) and 1 second pulses (CLK1HZ) are derived from a stable spacecraft oscillator and preconditioned by an FPGA aboard the master controller card as follows: they are one SCLK period in length, active low, and synchronized, transitioning with the rising edge of SCLK. This preconditioning assures that all DIFs are counting and reset in unison. The timing signals transmitted from the master controller to the event processing boards are below.

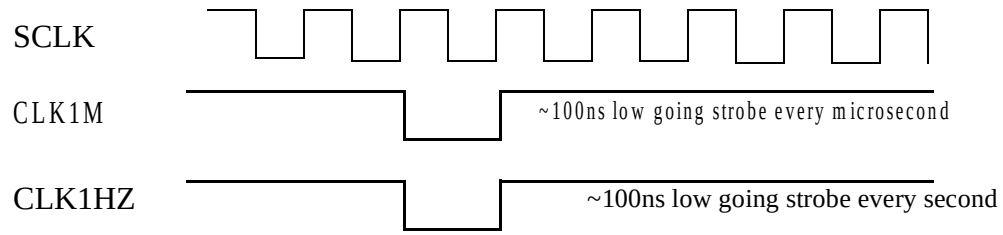

FIGURE 3. Clock and Timing Strobe Inputs

The real-time counter is a 10-bit synchronous counter which is reset by the 1 second tick (CLK1HZ) and clocked by the 1 MHz clock (CLK1M). The real-time count is passed onto the fast-rate counter module in order to time latch loading. It is also passed onto the event processing circuitry to serve as an event time tag.

3.0 AFE Power Shutdown

Two active high inputs (AFESHDN1:0), driven by the AFE power control circuitry, indicate an overcurrent condition in the AFE. If the Overcurrent Shutdown Enable is set (Register X0, Bit 3), a pulse (>1 microsecond) or high level on either AFESHDN1 or AFESHDN0 shuts down power to the AFE and sets an overcurrent detect register. The status of the overcurrent detect is returned

via the IDPU bus (Register XC, bit 2), which can be cleared by pulsing “Clear Latched Shut-down” (Register X7, Bit 0).

NOTE: the status bit is valid even when the Overcurrent Shutdown is disabled, allowing the CPU to read and reset Overcurrent Status without affecting AFE power.

AFE Power is controlled by the signal AFEPOW which is active high internal to the DIF, and inverted before it routed to the DIF output buffer. It therefore reads back as active high; the active low version controls the AFE power switch.

Overcurrent Shutdown Enable and Status are both cleared by RESET.

When the AFE power switch is off (default at RESET), all signals driven by the DIF to the AFE are held in a high-impedance state. These signals include:

DAC-DATA[11:0] - the DAC Data Bus (threshold and pulser DACs)
DITHER-DATA[5:0] - two separate 6-bit Dither DAC busses (Front and Rear)
PULSEOUT and PULSEOUTN
Pulser DAC Write Strobe
Threshold DAC Controls

4.0 Pulser Control

The Pulser Control Module generates a pulse of 10 microseconds at a programmable frequency. The frequency is programmable via Register X8 (see Section 1.1). The programmable 4 bit code translates to the following pulser frequencies:

Binary Code	Frequency
0000	Disable Pulser
0001	1 Hz
0010	2 Hz
0011	4 Hz
0100	8 Hz
0101	16 Hz
0110	32 Hz
0111	64 Hz
1000	128 Hz
1001	256 Hz
1010	512 Hz
1011	1024 Hz
1100 - 1111	Disable Pulser

There is additionally a disable bit in Register X1.

Both active high and active low versions of the pulse are available as DIF outputs.

Since the Pulser Module uses the time-base counter as its 1KHz timing reference, all generated pulses are synchronous to the 1 MHz S/C clock.

5.0 Monitor Rate Counters

The monitor rate counters clock upon detection of various pulses which are driven by the AFE. Four front detector pulses drive the Front Monitor Rate Counters and four rear detector pulses drive the Rear Monitor Rate Counters. (Additionally, the Live Time Count serves as a fifth Monitor Count Register. This section, however is contained in a separate module.)

Each monitor module consists of four ripple counters of varying widths, as specified in the HESSI IDPU Detector Interface FPGA Specification, Table 3.1-1. The bit count is repeated in Table 1,

Monitor Counter Name	Size of Counter	Bus Address	Comments
Front Preamp Reset	16 Bits	X4 - High Byte	Also causes CSA reset event
Front Slow Channel Valid Events	17 Bits	X4 - Low Byte	Falling edge clocks in event “VETO”
Front Slow Channel over ULD	9 Bits	X5 - High Byte	Also causes OverThreshold event and drives ULD for event VETO control
Front Fast Channel Valid Events	19 Bits	X5 - Low Byte	
Rear Preamp Reset	18 Bits	X6 - Low Byte	Also causes CSA reset event
Rear Slow Channel Valid Events	14 Bits	X7 - High Byte	Falling edge clocks in event “VETO”
Rear Slow Channel over ULD	8 Bits	X7 - Low Byte	Also causes OverThreshold event and drives ULD for event VETO control
Rear Fast Channel Valid Events	19 Bits	X8 - High Byte	

TABLE 1. Monitor Rate Counters

along with the associated bus address a summary of any other uses of the pulse within the DIF.

Each monitor counter module (Front and Rear) operates as follows: The four pulses are steered to the appropriate ripple counter. A state-machine (MCNTLSM) looks for the one second pulse. Upon its detection, it sequences the four count outputs through a 4:1 mux which drives a LOG19:8 compression module (LOGCOMP). (The specification for LOGCOMP follows Table 3.1-2 of the HESSI IDPU Detector Interface FPGA Specification.) The output of LOGCOMP feeds four 8-bit latches which are loaded in sequence by MCNTLSM. During this activity, MCNTLSM checks for Controller Card reads of the monitor counters, and blocks the latching if a read is detected. The busy period, which occurs once/second, has a duration of about 1 microsecond. During this time, all pulses into the monitor counters are ignored. All monitor counters are reset following a busy period.

Monitor rate inputs are pulses. Most are “Active-Low” which trigger the DIF with a falling-edge. The exception are the Fast Channel Valid Events, which are “Active-High” for both the front and rear detectors, and are thus rising-edge triggered.

If a monitor rate counter reaches its terminal count, the count is “locked-in” until reset following the one-second readout. In this event, the counters which are less than 19-bits will read back as Terminal Count+1 (log compressed into 8 bits), while the 19-bit counters will read back as the terminal count (or FFhex after the log compression).

See the BCF Functional Specification and the HESSI IDPU Telemetry Formats Description for more detail on the packetization of monitor rate register data.

6.0 Fast Rate Counters

The Fast Rate counters are four ripple counters and latches which track events from the AFE over specified timing intervals. They respond to four "active low" pulses: >E0, >E1, >E2 and >E3 (names shortened in the rest of this document to E0, E1, E2 and E3). The pulses signify energy threshold crossings and appear to the DIF as follows:

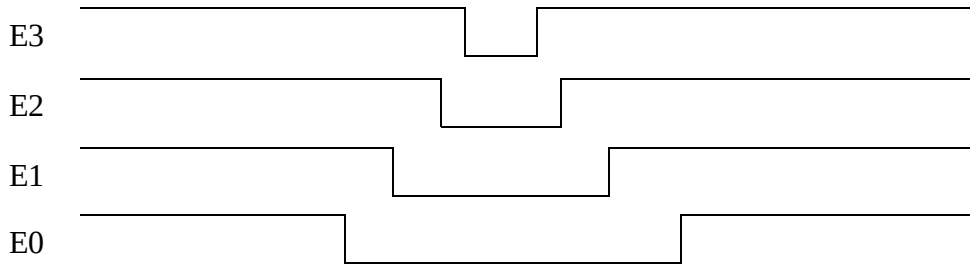

FIGURE 4. Fast Rate Counter Pulse Inputs

E0 is the minimum energy level required to trigger the lowest energy counter. The pulse circuitry (FRFFDEC) "wakes-up" upon detection of an E0 leading edge. The circuitry then latches any pulses from the remaining three energy levels, locking in the result at the trailing edge of E0. E0 is thus required for any of the other pulses to be recognized, although E1 - E3 are optional.

Two state machines operate in tandem to oversee the fast rate counters. FRESM generates count pulses to all four fast rate counters in response to a FEDET (falling edge detect) from FRFFDEC. FRFFDEC outputs an energy enable to each of the counters, which selects only one for any event. FRESM waits if the counters are about to be latched (in order to allow the ripple counters to settle.)

The state machine FRCNTSM loads the counters into the latches upon detection of a timing pulse. The timing pulse is derived from the central timing control counter, and selected by a decode circuit which looks at CARD-ID. HESSI IDPU DIF Specification, Table 3.2-1 specifies the sample rate required by each Card-ID. They are readout by the DIF into latches at the following frequencies: CARDIDs 0-2 at 16KHz, CARDIDs 3-5 at 4KHz and CARDIDs 6-8 at 1KHz. If FRCNTSM detects a read access to the fast rate counters, it waits one clock cycle before loading the latch.

A worst case stress on the Fast Rate Counter logic is the following scenario: FRESM is held up by FRCNTSM loading the latch, and FRCNTSM must wait due to a Controller Card read. This has been alleviated by one layer of pipelining in FRFFDEC. The recovery period between E0 pulses is 300ns: if two E0 pulses are separated by less than 300ns, the second one may not be registered.

The E0 pulse is synchronized to the 10MHz SCLK. Therefore the minimum pulse width (to guarantee recognition of E0) is 100ns. (Pulses shorter than 100ns may be counted if they arrive coincident with a SCLK rising edge.) The E1-E3 input registers, edge-triggered, will be set by any pulse which is higher than the Actel $V_{in\text{-}LOW}$ threshold. Thus the E1-E3 pulses can be arbitrarily small. However, these lines are noise sensitive: if there is activity on E1-E3 while E0 is deasserted, these counts will be registered when the next E0 arrives and activates FRCNTSM.

The counters range from 9 bits for the lowest energy counter, 8-bits for the two middle bins, and 7 bits for the highest energy counter. The sampling rate of the Fast Rate Counters is determined by the state of the CARD-ID as follows:

CARD ID	Number of Samples/Second	Formatting Mode
0,1,2	16K	16 bit mode
3,4,5	4K	32 bit mode
6,7,8	1K	32 bit mode

TABLE 2. Fast Rate Counter Mode Selection

The four output latches (32 bits) are formatted into two 16-bit words, depending CARD-ID. The resulting fast rate count readout appears at addresses X2 and X3 as follows:

Fast Rate Word	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
WORD 0 - Adr X2	C0 B8	C0 B7	C0 B6	C0 B5	C0 B4	C0 B3	C0 B2	C0 B1	C0 B0	C1 B7	C1 B6	C1 B5	C1 B4	C1 B3	C1 B2	C1 B1
WORD 1 - Adr X3	C1 B0	C2 B7	C2 B6	C2 B5	C2 B4	C2 B3	C2 B2	C2 B1	C2 B0	C3 B6	C3 B5	C3 B4	C3 B3	C3 B2	C3 B1	C3 B0

TABLE 3. Fast Rate Counter Readout - 32 bit mode

Fast Rate Word	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
WORD 0 - Adr X2	C0 B4	C0 B3	C0 B2	C0 B1	C0 B0	C1 B3	C1 B2	C1 B1	C1 B0	C2 B3	C2 B2	C2 B1	C2 B0	C3 B2	C3 B1	C3 B0

TABLE 4. Fast Rate Counter Readout - 16 bit mode

where C0 through C3 signify counters 0 through 3, and B8 through B0 signify the counter bits.

The Fast Rate Counters freeze upon reaching their terminal counts until latched and reset at the by the CARD-ID dependent timing tick. CARD-IDs 0, 1 and 2 (16 bit mode) counters freeze at the abbreviated terminal count, dependent on the number of counter bits allocated to telemetry. (For instance counter 0 freezes at 511 (decimal) in 32 bit mode and at 31 (decimal) in 16 bit mode.)

7.0 Live Time Counters

There are two live-time counters, both 20-bit ripple counters clocked by CLK1M and reset (and latched) by CLK1HZ. Each counter is dedicated to logging the proportion of active event processing time for a detector.

Both the rear and front analog front-ends forward a signal to the DIF which represents the signal processing “dead-time”. This signal goes low when the analog front-end is “busy”; a low therefore disables the corresponding live-time counter. Additionally, two internal DIF signals (Front and Rear), active when the IDPU I/F circuitry is busy waiting, can also inhibit live-time counting. The upper 8-bits of the live-time counters are latched once/second are available via the bus interface.

Each 20-bit ripple counter “freezes” when the upper 12-bits are set (the maximum read-out count).

The combined livetime inhibit for each detector is forwarded back to the event processing modules in order to gate the 2KHz live time counter modules.

8.0 Event Processing

The front and rear event processing sections are almost identical. Exceptions are mentioned in Section 8.5 on page 16. Front and rear modules both contain: an event detection/controller state machine, latches to store time and energy data, a rejected events counter, and an “event adjust” module. A schematic of the Rear Detector Event Processing Module is shown in Figure 5 below.

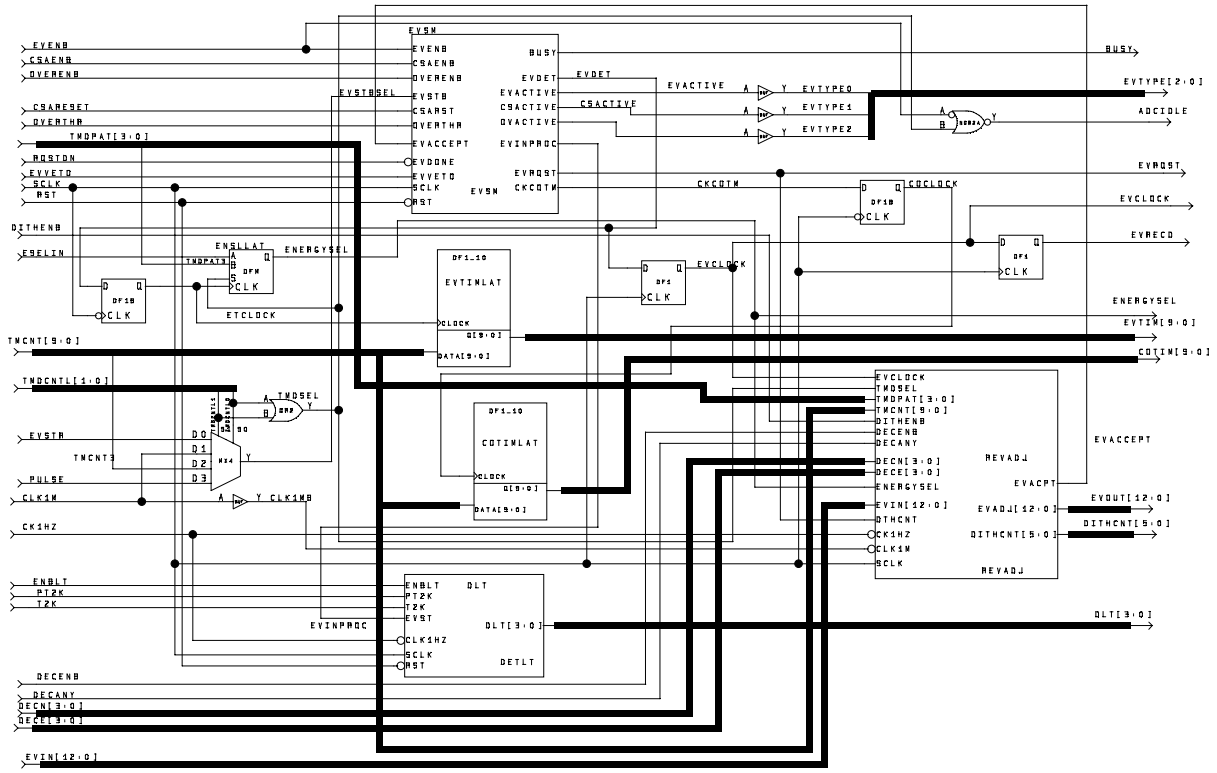

FIGURE 5. Event Processing Module (Rear)

The enables can be seen on the left as inputs to the Event Processing State Machine module (EVSM). On the lower left (DLT) is the 2KHz live time counter module, which accumulates detector live time between 2 KHz ticks and telemeters the result as part of the event word. The event adjust module, discussed below, determines if an event is included in the telemetry stream and adds a “dither” offset.

8.1 Event State Machine (EVSM)

The event state machine looks for pulses on the Event Strobe, the CSA Reset Signal and the Over-Threshold Signal from the AFE. If more than one signal arrives simultaneously, it prioritizes them as follows: Events, CSA Reset and OverThreshold. The state machine latches in the type of cycle and requests the bus controllers attention. It then freezes access (locks out events which might arrive during this Busy-Wait period). The bus controller, which handles the transfer of event data to the IDPU, informs the event state machine when the event transfer has completed. This allows the reception/transfer of the next event. A “BUSY” signal (asserted only if an event arrives while the a preceeding event is still awaiting a bus controller “DONE” signal) is for-warded to the live-time counters (see Section 8.0- Live Time Counters) which inhibits counting.

Any type of event can be disabled for each detector independently via the Enables register (see Section 1.1) or the Event Veto Controller.

8.2 Latches

Upon reception of an event strobe, event energy data and time are latched (see EVINLAT in Figure 6). In order to adjust for the 2's-complement output of the ADC, the lower 12 event bits are inverted by the energy input latch after the dither offset has been added to the 13-bit ADC data.

A separate latch is maintained for CSA Reset and OverThreshold Pulse processing time. This allows an event to be accurately time-stamped while a CSA Reset or OverThreshold bus transfer is in progress. Note that the CSA Reset and OverThreshold Events are timestamped at the time of service, which may be microseconds (depending on the backlog of the Master Bus controller) later than the time of arrival.

Because the event latching is synchronized to the system clock, event data must be held to within 2 clock pulses after the rising edge of the event strobe. This imposes a 250ns hold-time requirement. The required event data setup time is 50ns.

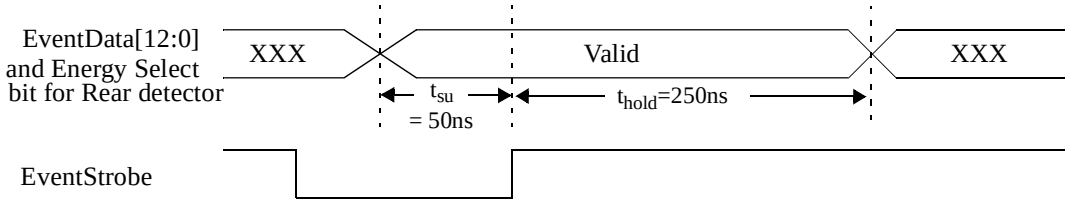

TABLE 5. Event Data and Strobe Timing Requirements

The falling edge of the event strobe is not used by the DIF. (EventStrobe is the “BUSY” output of the LTC1604, the AFE analog-to-digital (ADC) converter.)

8.2.1 ADC and Event Veto Control

The ADC used by the AFE (LTC1604) is held in “nap” mode between conversions by driving the (SHDN) low. The DIF receives “start discriminator” signals from each detector (FSD and RSD) which cause the SHDN outputs to be driven high, in anticipation of an upcoming conversion. Following the detection of a rising edge on either EventStrobe, the corresponding SHDN signal is again driven low.

The ADC control state machine is also used to “wake-up” an event veto controller. When the ADC is active, a “VETO” latch, clocked by the falling edge of the SLCHANVAL monitor rate pulse (also known as the ADC “CONVERT” signal), captures the state of the SLCHANOVR monitor rate (also known as the ULD signal). VETO, which blocks the associated EventStrobe (ADC “BUSY” output) before the event processing state machine can see it, is cleared when the ADC returns to “nap” mode.

8.3 2 KHz Live Time Counters

Each event processing module contains a 9-bit ripple counter, which accumulates detector live time, counting at 1 MHz and gated by both detector live time and DIF “bus busy” based live time signals. (See Section 7.0, “Live Time Counters,” on page 12.)

The counter is latched and then reset at approximately 2KHz (CLK1M x 2^9), synchronous with the S/C 1 Hz clock. At the 2KHz tick, the latched information is transferred into the telemetry stream via the next three event words, using the following format:

Following 2KHz Tick	Live Time Nibble Format
First Word	1, CNTR8, CNTR7, CNTR6
Second Word	0, CNTR4, CNTR4, CNTR3
Third Word	0, CNTR2, CNTR1, CNTR0
Following Words until next 2KHz Tick	0,0,0,0

Once the first word is read-out, the latch is “frozen” until the measurement is completely telemetered, although the counter continues to reset at every 2KHz tick. If the first word has not yet read-out, or all three values have been read-out, a new value overwrites the previously latched count.

8.4 Event Adjust

The event adjust module contains a dither counter (6 bits), a decimation counter (4 bits), a 12 bit adder and a four bit magnitude comparator.

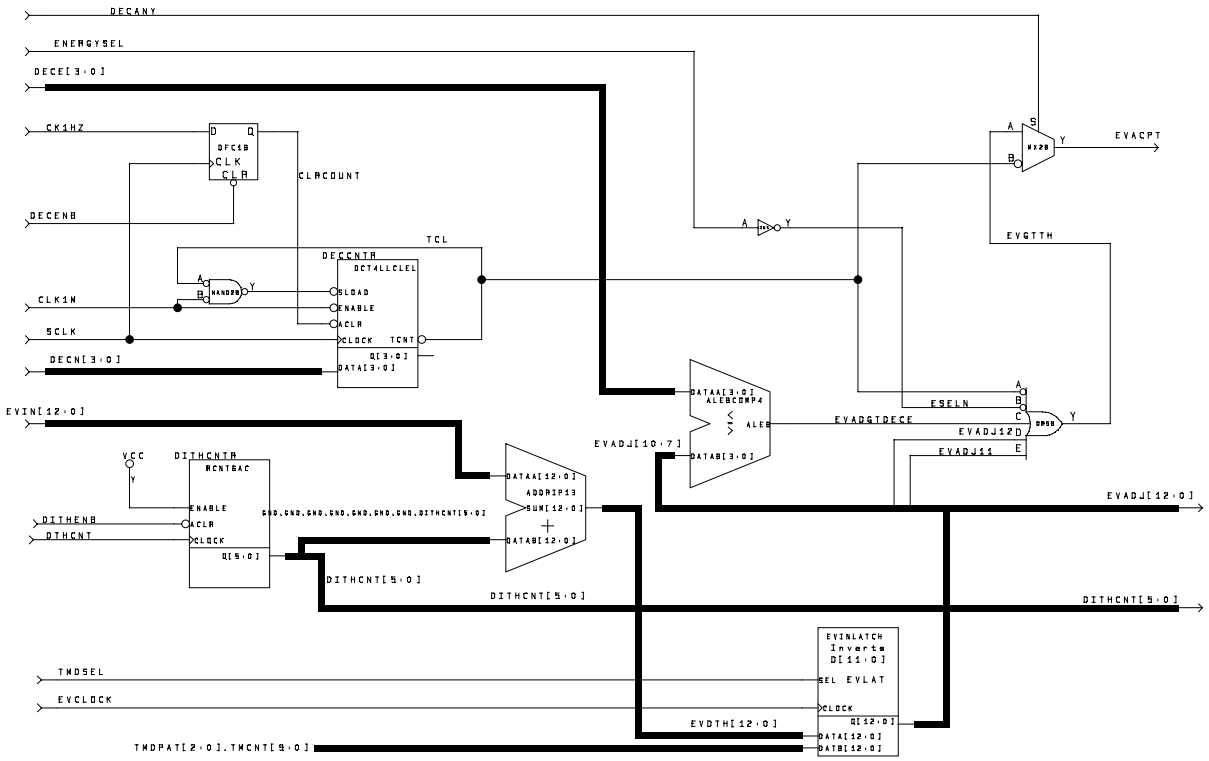

FIGURE 6. Event Adjust Module (Rear)

The dither counter clocks following each event read out by the IDPU. (Not all events qualify for read-out as explained below.) The dither count is output to the AFE in order to offset the A/D, and it is also added to the event in process. The resulting value (Event + Dither Count) is then partially inverted (the MSB of the 13 bit ADC word and the Rear Energy Select bit are not inverted), latched and "decimated."

The decimator accepts events based on either a slice of time, or event energy. It can be set up to compare 4 critical bits of the event energy word to determine if an event qualifies. For the rear detector, shown above in Figure 6, the energy comparison looks at bits 7-10 (bits 11, 12 and the EnergySel bit must be 0 for and event to be rejected) and compares them to the programmed energy threshold. The front detector event adjust module looks at bits 4-7 (bits 8-12 must be 0 for the event to be rejected). The energy parameter is set via a DIF bus register (Decimation Parameters, see Section 1.1). An additional option bit, contained in the Enables Register, instructs the decimator to decimate any event.

The Decimation time slice, also set via the Decimation Parameters register, sets the interval for which all events are accepted. The 4-bit count value establishes a terminal count; when the terminal count is reached, the decimator accepts any event regardless of energy.

Both decimation and dithering can be disabled via the Enables Register.

8.5 Rear vs. Front

The rear detector processing differs from the front in the following ways:

Decimation looks at different energy bits (see above section)

An energy select bit is latched, used in the decimator, and forwarded to the event formatter.

9.0 Event Formatter

The event formatter, a purely combinatorial module, inputs events information from both the rear and front event processing modules and assembles a formatted 32-bit word based on the active detector, and the event type. CARD-ID is used to generate the Source Code and Detector ID fields (see the HESSI IDPU Detector Interface FPGA Specification) for a list of Source Codes, and the description of the formatted event words. The readout format (at bus address X0-X1) is shown below:

Event Word	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
WORD 0 - Addr X0	S4	S3	S2	S1	S0	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2
WORD 1 - Addr X1	E1	E0	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	L3	L2	L1	L0

TABLE 6. Event Readout Format - Energy Based Events

Event Word	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
WORD 0 - Addr X0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	X	X	X	X	X	X
WORD 1 - Addr X1	X	X	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	X	X	X	X

TABLE 7. Event Readout Format - CSA Reset and Over Threshold Events

where S represents source code, D detector ID, E event energy, T time stamp, L 2 KHz live time accumulation and X unused bits. See the HESSI IDPU Detector Interface FPGA Specification for further detail.

10.0 Output Mux

A simple 10 to 1 by 16 bit output mux serves as the final DIF output selection for data being read by the Master Controller card. The select bits are driven by the IDPU address bits 0-3. A matching CARD-ID in the upper four address bits enables data from the DIF onto the IDPU data bus. The readout decode follows the address map shown in Section 1.1, “Bus Registers,” on page 5.

11.0 Test Mode

Test mode was added to in order to fully exercise the event processing circuitry without an analog stimulus present. During test-mode, the A/D input latches are bypassed; event data is injected from a combination of two sources. The 10-bit time stamp (TMCNT[9:0]) feeds the lower 10 bits, and a 4 bit parameter register field (the test mode parameter field) supplies the upper three bits of front event data and the upper four bits of rear event data. (The most significant bit sets the Rear Energy Select bit.)

Since the lower 12-bits of the event are inverted by the energy input latch, most of the test mode data will be inverted prior to the EVADJ stage. The lower 10 bits of the event are the inversion of the TMCNT[9:0]. The next two bits are the inversion of the two LSBs of the 4 bit parameter field. The upper energy bit and Rear Energy Select bit (MSBs of the parameter field) are not inverted.

The event strobe during test mode is determined by the test mode control field as follows:

00 => Normal (test mode disabled)
01=> 1 MHz Clock = Event Strobe
10=> 62.5 KHz Clock = Event Strobe
11=> Pulser Output = Event Strobe

For information regarding the pulser output, see Section 4.0 on page 9.

Decimation can be adjusted during testmode in the same manner as for normal operation. Since dithering occurs prior to the latching of ADC data, test mode data does not include the dither counter offset; however the dither counter will clock if dithering is enabled. Parameters and control bits are initialized via the DIF register interface (see Section 1.0 on page 3). Reset clears the test mode control and parameter fields.