HESSI IDPU to ADP Interface Control Document

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1. Introduction

This document is a specification for the interface between the HESSI Instrument Data Processing Unit (IDPU) and the Aspect Data Processor (ADP). The ADP is a board that fits into the IDPU VME rack. This board interfaces with the aspect sensors (RAS and SAS), processes the aspect data, and formats it for inclusion in the science telemetry stream. The aspect sensors and ADP are provided by PSI, while the remainder of the IDPU is provided by U.C.Berkeley.

1.1 Related Documents

These documents are available on the web at:

ftp://apollo.ssl.berkeley.edu/pub/hessi/

[1] HESSI IDPU Backplane Signals (HSI_SYS_019)
[2] HESSI IDPU VME Card Specification (HSI_IDPU_011)
[3] HESSI IDPU VME Chassis ICD Drawing (HSI_SYS_011)
[4] HESSI Instrument Harness Specification (HSI_SYS_022)
[5] HESSI Telemetry Formats Document (HSI_SYS_007)
[6] HESSI Command Formats Document (HSI_SYS_008)
[7] HESSI IDPU to Spacecraft ICD (HSI_SYS_001)
[8] HESSI ADP Telemetry Formats (HSI_SYS_032)
[9] HESSI ADP DSP Software Requirements (HSI_ADP_001)

2. Board Layout Issues

The ADP board shall have a 6U-VME card form factor with a single P1 backplane connector as shown in reference 2. The pinout of the P1 connector is called out in reference 1. Three front panel connectors interface with the RAS and SAS via IDPU-J7 and IDPU-J8, as well as the Ground Support Equipment via IDPU-J9. The location of these connectors is shown in reference 3, and the pinouts in reference 4.

The edges of the card are held in the chassis by wedgelocks indicated in reference 2. Spacers are required between the board and the wedgelock on the component side of the board and also on the solder side of the board to fit into the card guide of the IDPU chassis. These spacers and wedgelocks shall be provided by UCB.

A shield board must be attached to the ADP to provide RF shielding in the IDPU chassis and to provide added stiffness to the board. This shield board shall be made from 0.034" PCB material plated on one side, and attached to the solder side of the ADP via 0.100"-0.125" spacers and screws. At least one of these screws must connect the shield board plated side electrically to ground on the ADP. The dimensions of the shield board shall

be the same as the ADP board (as indicated in reference 2), less 0.4" on each side to avoid the card guides.

3. IDPU Backplane Interface

The IDPU backplane is specified in Reference 1. Table 3-1 indicates the addresses of registers accessible via the IDPU backplane.

Loading of the bus signals should be minimized, and BUSCLOCK in particular may drive only one input on the ADP.

Table 3-1 Register Addresses

Address (Hex)	Read / Write	Register Name	Contents
91	R	ADP_FIFO	High speed telemetry interface FIFO access
95	R/W	ADP_PSR	Power Switch Register
97	R/W	ADP_PSRE	Extended Power Switch Register
96	R	ADP_PER	Power Error Register (service overcurrent sense)
94	R	ADP_ICR	Interface Control Register
90	W	ADP_MCR	Message Command Register
92	R/W	ADP_MDR	Message Data Register
93	R	ADP_MSR	Message Status Register
9F	W	ADP_RESET	DSP Reset
F0	W	AHKP_SELECT	See Reference 1 and Section 3.2.
FE	W	TCW1	Time Code Word MSB. See reference 1
FF	W	TCW0	Time Code Word LSB. See reference 1.

3.1.1. High Speed Telemetry Interface (ADP_FIFO)

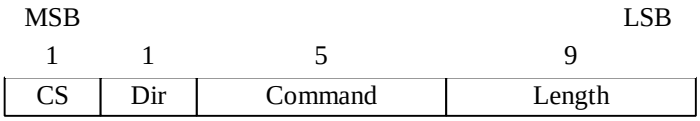
The IDPU Data Controller shall automatically collect ADP science telemetry from the ADP_FIFO register in response to a request signal from the ADP as described in reference 1. The IDPU software should not access this register while the ADP telemetry is active (this would cause the system to lose synchronization). Telemetry shall be transferred in packets as described in Reference 5. The specifics of the ADP packets are described in reference 8.

3.1.2. Message Interface

Most ADP commands and non-science data are transferred via the message interface. Transfers are initiated by the IDPU writing to the ADP_MCR, followed by a read of the ADP_MSR. The MSR should be read no sooner than 36µs after the ADP_MCR is written to allow time for the ADP to process the command. If the ADP_MSR indicates an error (Busy, ME, or Rdy high), the transfer shall be aborted and an error shall be indicated in the State-Of-Health (SOH) telemetry. For multiple-word transfers, a series of transfers to/from the ADP_MDR follow on intervals no less than 36µs. The type and

direction of a message is indicated in the ADP_MCR transfer. The formats for the ADP_MCR and ADP_MSR registers are shown in figure 3.1.2-1 and 3.1.2-2.

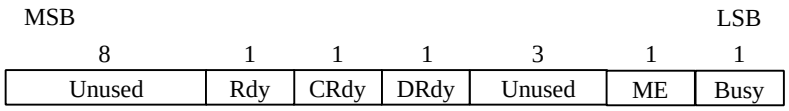
Figure 3.1.2-1 ADP_MCR Register Format



- CS is a parity code for the command: the sum of the bits in a valid ADP_MCR, including CS, should be odd. For example, ADP_MCR = 8000 is a valid command.
- Dir indicates the direction of the following data words:
  - Dir = 0 means the IDPU will write the data words to the ADP_MDR
  - Dir = 1 means the IDPU will read the data words from the ADP_MDR (the ADP will provide the message data)
- Command indicates the type of message being transferred (see below for command codes)
- Length is the number of data transfers to the ADP_MDR (1 to 512 16-bit words; limited to no more than 64 by IDPU transfer timing constraints)

Command = 0 with Dir = 0 is a special case of a "no-data" message. No ADP_MDR transfers will follow, and the Length field contains an extended command code.

Figure 3.1.2-2 ADP_MSR Register Format



- Rdy (Ready) is the logical OR of Drdy and Crdy. These signals should go active when the transfer is made by the IDPU, and should go inactive within 36µs.
- CRdy (Command Ready) = 1 means that the ADP hardware has received a command (via ADP_MCR) which it has not yet been picked up by the DSP.
- Drdy (Data Ready) = 1 means that the ADP hardware has received a data word (via ADP_MDR) which it has not yet been picked up by the DSP.
- ME (Message Error) =1 means the ADP detected an error in the message format (bad CS, bad command code, etc.). This bit should normally be zero. This signal is set within 36µs of receipt of the bad command via the ADP_MCR, and is reset when the ADP_MSR is read.
- Busy =1 means the ADP is not ready to receive messages. Normally this bit should be zero within 36µs of receipt of a command via the ADP_MCR.

A list of command codes is indicated in table 3.1.2-1.

Table 3.1.2-1 Message Command Codes

Code (Decimal)	Read / Write	Length / Extended Code	Command Name	Comments
0	W	0	ADP_STOP	Stop processing data in preparation for a parameter or other change
0	W	1	ADP_INIT	Re-initialize ADP system
0	W	2	ADP_STE	SAS Telemetry Enable (*)
0	W	3	ADP_STD	SAS Telemetry Disable (*)
0	W	4	ADP_RTE	RAS Telemetry Enable (*)
0	W	5	ADP_RTD	RAS Telemetry Disable (*)
0	W	40	ADP_TPM	ADP test program memory(diag)
0	W	41	ADP_TPM	ADP test data memory(diag)
0	W	42	ADP_TPM	ADP test FIFO memory(diag)
1	W	1	ADP_ADDR	Set the read address for ADP_PFR, ADP_HSR, ADP_RTR, ADR_MR, and ADO_PR
2	W	1	ADR_RUN	Run ADP Program (parameter is the program number to run)
3	R	20	ADP_SOHR	Read ADP SOH data
4	R	8	ADP_ACSR	Read ADP ACS Aspect solution
5	R/W	N	ADP_PTR ADP_PTW	Read/Write N words to the current ADP Parameter Table
6	R/W	N	ADP_HSR ADP_HSW	Read/Write N words to the current ADP Hot Spot Table
7	R/W	N	ADP_RTR ADP_RTW	Read/Write N words to the current to ADP RAS Threshold Table
8	R/W	N	ADP_PMR ADP_PMW	Read/Write N words to the current ADP Program memory
9	R/W	N	ADP_MR ADP_MW	Read/Write N words to ADP Memory
10	W	1	ADP_PTEW	Write current ADP Parameter Table to EEPROM table (parameter = EEPROM table #)
11	W	1	ADP_HSEW	Write current ADP Hot Spot Table to EEPROM table (parameter = EEPROM table #)
12	W	1	ADP_RTEW	Write current ADP RAS Threshold Table to EEPROM table (parameter = EEPROM table #)
13	W	1	ADP_PMEW	Write current ADP Program to EEPROM table (parameter = EEPROM table #)
14	W	1	ADP_PTER	Read ADP Parameter Table from EEPROM into current (parameter =

				EEPROM table #)
15	W	1	ADP_HSER	Read ADP Hot Spot Table from EEPROM into current (parameter = EEPROM table #)
16	W	1	ADP_RTER	Read ADP RAS Threshold Table from EEPROM into current (parameter = EEPROM table #)
17	W	1	ADP_PMER	Read ADP Program from EEPROM into current (parameter = EEPROM table #)
18	TBD			TBD
19	R	N	ADP_GTRES	Get test data (diag)
20	R/W	N	ADP_IOR ADP_IOW	Read/write I/O memory
21	R/W	N	ADP_BEPR ADP_BEPW	Read/write Program eeprom
22	R/W	N	ADP_PEPR ADP_PEPW	Read/write parameter eeprom
23	R/W	1	ADP_BPVR ADP_BPVW	Read/write boot program version
24-31				Unused

(*) - These telemetry enable/disable commands control two flags; RAS_TLM_EBL, and SAS_TLM_EBL. Telemetry is enabled only if both the Parameter Table enable for the sensor and and this enable are both active. RAS_TLM_EBL and SAS_TLM_EBL shall default to Enabled on reset, and should be reported in the ADP SOH telemetry.

The memory/table write commands (code 5-9, Write) include an embedded address (formatted into the block as part of the command packet on the ground) in the first data word, which is the address to start loading the following data to. This allows large tables to be loaded in several commands, or individual pieces or arbitrary size to be modified. The format of the words transferred to the MDR for these messages is shown in table 3.1.2-2.

Table 3.1.2-2 Memory/Table Load/Dump Format

Word Number	Contents
1	IDENTIFIER
2	ADDRESS *
3	LENGTH
4 - LENGTH+4	LENGTH-1 Data words to load

* - ADDRESS is an absolute address for Memory and Program loads, and a relative address for table load commands (from the start of the table).

The memory/table read commands (code 5-9, Read) shall also include a header (added by the ADP) using the same format described in Table 3.1.2-2. If a memory/table read command is preceded by an ADP_ADDR command, this is used as the address to read

from. Otherwise, the ADP will continue from wherever reading for that memory or table was last read from.

3.1.3. Power Control

The ADP has power switches and current limiters for the RAS, 3 SAS sensors, and the DSP power services. The power switches are controlled by the IDPU via the ADP_PSR and ADP_PSRE registers. The bit allocation of the switch settings in this register is shown in table 3.1.3-1 and 3.1.3-2. A zero in this register means ON, and a one means OFF. A bus reset turns these switches. The ADP_PSR and ADP_PSRE can also be read by the IDPU.

The ADP_PER is a read-only register that indicates the current limiter status on each supply. The bit allocations are shown in table 3.1.3-3. A zero indicates that the supply is OFF, either because the associated PSR bit is set to OFF, or because of an over-current condition.

The IDPU software shall be designed to turn on or off all control bits of a subsystem (such as RAS or SAS1) together.

Table 3.1.3-1 ADP_PSR Register Format

Bit	System	Voltage
0 (LSB)	RAS	+15V
1	SAS1	+15V
2	SAS2	+15V
3	SAS3	+15V
4	RAS	+12V
5	SAS1	+12V
6	SAS2	+12V
7	SAS3	+12V
8	RAS	+5V
9	SAS1	+5V
10	SAS2	+5V
11	SAS3	+5V
12	Unused	
13	Unused	
14	Unused	
15 (MSB)	Unused	

Table 3.1.3-2 ADP_PSRE Register Format

Bit	System	Voltage
0 (LSB)	RAS	+5V Digital
1	SAS1	+5V Digital
2	SAS2	+5V Digital
3	SAS3	+5V Digital

4	DSP	+5V Digital (vcc1)
5	SRASI/F	+5v Digital (vcc)
6	Unused	
7	Unused	
8	Unused	
9	Unused	
10	Unused	
11	Unused	
12	Unused	
13	Unused	
14	Unused	
15 (MSB)	Unused	

Table 3.1.3-3 ADP_PER Register Format

Bit	System	Voltage
0 (LSB)	RAS	+15V
1	SAS1	+15V
2	SAS2	+15V
3	SAS3	+15V
4	RAS	+12V
5	SAS1	+12V
6	SAS2	+12V
7	SAS3	+12V
8	RAS	+5V
9	SAS1	+5V
10	SAS2	+5V
11	SAS3	+5V
12	RAS	+5V Digital
13	SAS1	+5V Digital
14	SAS2	+5V Digital
15 (MSB)	SAS3	+5V Digital

Note there is no overcurrent indication for the DSP +5V Digital; this should be monitored via the analog housekeeping IADP_P5D1V, IADP_P5D2V, and IADPD3V (threshold = 4 volts).

3.1.4. ADP Interface Control Register (ADP_ICR)

Writing this register by the IDPU sets interface controls, as indicated in table3.1.4-1.

Table 3.1.4-1 ADP_ICR Register Format

Bit	Name	Description
0 (LSB)	Rdy	Same as MSR bit 7.
1	IRQM	Interrupt Mask
2	-	Unused

3	-	Unused
4	-	Unused
5	ADPSOP	Status of ADPSOP interface signal (related to high speed science data transfers)
6	-	Unused
7	ADPTR	Status of ADPTR interface signal (related to high speed science data transfers)
8	-	Unused
9	-	Unused
10	-	Unused
11	-	Unused
12	-	Unused
13	PER	Power Error (OR of PER bits)
14	FAR	FIFO Access Error; a one indicates a request has been made to read the FIFO when no data is present.
15 (MSB)	ERROR	This is a combined error flag, which is a logical OR of the PSR, MSR, and ISR error conditions (a 1 indicates an error).

3.1.5. ADP DSP Reset (ADP_RESET)

A write to this register with the LSB set to 1 will cause the ADP DSP and associated logic to be reset. It will remain reset until this register is re-written with the LSB set to 0. The IDPU shall hold reset active for at least 10µs. If bit 1 in this register is zero during the reset, the DSP shall start executing the first boot program in the EEPROM. If bit 1 is 1 during the reset, the DSP shall start executing the next boot program in EEPROM. For example, a reset with bit 1 set to 0, followed by 2 resets with bit one set to 1 will cause the DSP to execute the third boot program in EEPROM. The status of which boot program is being run shall be included in the ADP SOH data.

3.2. *Analog Housekeeping*

The IDPU backplane has a single analog signal that is shared by all the VME cards and measured by an ADC on the Data Controller card. The ADP shall have a tree of analog H508A multiplexers driving that line, and addressed by the AHKP_SELECT register as described in reference 1. When the AHKP_SELECT register is set to a value outside the range for the ADP (90-AF), the output of the multiplexer(s) on the backplane analog bus should be disabled so another card can drive it.

The inputs to the tree shall not exceed +/- 2.5V , and shall have a source impedance of < 50kohms. . Capacitance on the analog bus should be minimized.

Table 3.2-1 describes the analog measurements, how they are scaled, and appropriate alarm limits for the ground system. The monitors are all voltages, and the "Scale" factor is the divider applied to the voltage to get it into the range of +/-2.5V.

Table 3.2-1 Analog Housekeeping Measurements

AHKP _Select	Signal	Measurement	Scale	Limits
90	IRAS_P15V	RAS +15V Monitor	0.1483	
91	ISAS1_P15V	SAS #1 +15V Monitor	0.1483	
92	ISAS2_P15V	SAS #2 +15V Monitor	0.1483	
93	ISAS3_P15V	SAS #3 +15V Monitor	0.1483	
94	IRAS_P12V	RAS +12V Monitor	0.1483	
95	ISAS1_P12V	SAS #1 +12V Monitor	0.1483	
96	ISAS2_P12V	SAS #2 +12V Monitor	0.1483	
97	ISAS3_P12V	SAS #3 +12V Monitor	0.1483	
98	IRAS_P5V	RAS +5V Monitor	0.4087	
99	ISAS1_P5V	SAS #1 +5V Monitor	0.4087	
9A	ISAS2_P5V	SAS #2 +5V Monitor	0.4087	
9B	ISAS3_P5V	SAS #3 +5V Monitor	0.4087	
9C	IADP_P5D1V	DSP +5V Digital Monitor #1	0.4087	
9D	IADP_P5D2V	EEPROM+5V Digital Monitor #2	0.4087	
9E	Unused			
9F	Unused			
A0	IRAS_P5DV	RAS +5V Digital Monitor	0.4087	
A1	ISAS1_P5DV	SAS #1 +5V Digital Monitor	0.4087	
A2	ISAS2_P5DV	SAS #2 +5V Digital Monitor	0.4087	
A3	ISAS3_P5DV	SAS #3 +5V Monitor	0.4087	
A4	IADP_P5D3V	SAS RAS I/F +5VD Monitor	0.4087	
A5	IADP_FPGA	ADP-IDPU I/F FPGA +5V Digital Monitor	0.4087	
A6	Unused			
A7	Unused			
A8	Unused			
A9	Unused			
AA	Unused			
AB	Unused			
AC	Unused			
AD	Unused			
AE	Unused			
AF	Unused			

4. IDPU Software Requirements

The IDPU software controls all interactions with the ADP over the backplane. The collection of data from the ADP_FIFO register in response to an ADP_ETR request (as described in reference 1) is handled automatically by the IDPU hardware, but the IDPU software still controls the enabling of this at the IDPU end. All other transactions are handled explicitly by the IDPU software using I/O instructions directly mapped into the ADP registers described in table 3.1.

4.1. *Analog Housekeeping*

The IDPU shall sample all ADP housekeeping values indicated in Table 3.2-1 approximately once a second and include these values in the State-of-Health (SOH) packets sent to the spacecraft. All samples shall be encoded as 8-bit values (7 bits plus sign) covering the range +/-2.5V linearly. The IDPU shall perform no other operations on these values.

4.2. *Power Control*

The IDPU shall decode and implement a ground command to set the ADP_PSR and ADP_PSRE registers. The value programmed into this register shall be included in the SOH packet. The IDPU shall also monitor the ADP_PER register once a second.

In the event of a power error, the IDPU shall automatically turn off all switches associated with the subsystem that has a supply error via the ADP_PSR and ADP_PSRE registers. A map of ADP_PER / ADP_PSR bits to subsystem is shown in section 3.1.3. The IDPU shall also report this error in the SOH data. The IDPU shall attempt to turn the subsystem back on after a delay of at least 4 seconds. If the subsystem again shuts down (as indicated in the ADP_PER), the IDPU shall attempt to turn it back on no more than 5 times before abandoning the attempt and leaving the subsystem off.

4.3. *ADP Reset*

The IDPU shall decode and implement a ground commands to reset the ADP (via the ADP_RESET register). One command shall reset to the first ADP boot program, while a second shall reset to the next ADP boot program (see 3.1.5).

4.4. *ADP Instrument Control*

The ADP_ICR register shall be read back and included in the SOH data.

4.5. *Command Packets*

In addition to the commands described in section 4.2-4.4, the IDPU shall decode ground command packets with an application-ID 1026, indicating the ADP and pass them on to the ADP via the messaging system described in section 3.1.2. The command code shall be copied from the command packet function field. The command length shall be computed from the packet .

The IDPU will provide Ap-ID 1024 commands to implement "no-data" commands.

To read from the ADP, the ADP_ADDR command will be sent to the ADP, setting the address for the transfer. The IDPU will be commanded to dump 'X' ADP diagnostic packets of type 'T' (T is the command code used, 5-9, as indicated in table 3.1.2-1). The IDPU will perform 8 reads of 128 bytes per second to fill Diagnostic packets (until X packets have been transferred).

The IDPU shall be capable of controlling the power (via the ADP_PSR and ADP_PSRE registers) and telemetry enable (via the RAS and SAS telemetry enable messages) as the spacecraft transitions in and out of eclipse. This may be done automatically, in response to the eclipse signal from the spacecraft, or by time-tagged command. The sequence of commands shall be programmable, so that the decision of what systems to enable/power-off in eclipse can be made after launch, in response to power and telemetry budget considerations.

4.6. *Digital SOH collection*

The IDPU shall collect one 40-byte block of SOH data from the ADP each second using ADP_SOHR. This transfer shall occur synchronous to the CLK1Hz signal, no sooner than 100us and no later than 500ms after the CLK1Hz signal. The data will be collected using a ADP_SOH message as indicated in section 3.1.2-1. The IDPU shall pass this information on to the spacecraft in the SOH block during the following 1-second interval. No further operations shall be performed on this data by the IDPU. The format of this data is TBD-PSI.

4.7. *On-board SAS Aspect Solution Collection*

The IDPU shall collect one 16-byte block of SAS Aspect Solution data from the ADP each second using ADP_ACSR. This transfer shall occur synchronous to the CLK1Hz signal, no sooner than 100us and no later than 500ms after the CLK1Hz signal. The data will be collected using a ADP_SAS message as indicated in section 3.1.2-1. The IDPU shall pass this information on to the spacecraft during the following 1-second interval. No further operations shall be performed on this data by the IDPU. The format of this data is indicated in reference 7. If the ACS data transfer fails, the IDPU will mark the data passed to the spacecraft as invalid.