

HESSI Data Controller Board Test Sequence

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Test Unit: _____

Test Date: _____

Tested By: _____

1. Overview

This document describes the HESSI IDPU Data Controller Board (DCB) test sequence. This sequence shall be performed on the flight DCB prior to mating with other flight hardware. This test sequence shall provide a functional verification of all DCB functions.

2. Handling Issues

The flight DCB shall be handled with appropriate precautions to ensure high reliability. The board shall be handled only with clean gloves, and shall remain bagged or boxed in clean ESD-protected environment when not in use. An appropriately grounded ESD wrist-strap shall be used while handling the DCB, and gloves shall be periodically grounded to avoid charge build-up.

Probing on the flight hardware is to be minimized. Oscilloscope probes and other relatively heavy test probes that can stress component leads shall not be clipped directly to flight component leads.

3. Test Equipment

The testing shall involve the following equipment and software:

1. ETU IDPU backplane and VME chassis
2. Power supplies (bench supplies)
3. Spacecraft simulator GSE (interface box, PC, and scgse3c.exe, scgse5e.exe, and ssr.exe, plus ADCDCBRamp.exe)
4. ROM emulator with special harness to connect to DCB
5. DCB test board (plugs into IDPU-J6)
6. DCB test software (test.a)
7. Break-out box
8. ETU ADP & DIB boards
9. Tail pulser (Berkeley Nucleonics), Oscilloscope, Volt meter

4. Pre-Test Inspection

The DCB shall be inspected by QA following fabrication, and prior to the start of testing to verify appropriate workmanship levels. This shall be indicated in the flight DCB log book.

Prior to testing, the DCB shall be inspected to verify the following:

1. All components are installed, except U5 (PROM, socketed), Y2 (unused oscillator), and the spare DIP: _____
2. Actel version numbers: BCF: _____ PFF: _____

3. Tantalum capacitors, diodes, and ICs are installed with the correct polarity according to the silk-screen on the PWB (with the exception on C58, which is marked incorrectly on the silk screen): _____
4. JP1 is not installed, JP2 has a jumper between pins 1&2: _____
5. The fix to U30 (IDPU-DCB-PWB-012) has been completed: _____

5. Initial Power On Test

5.1. Configure DCB:

- Install DCB into VME chassis with ETU IDPU backplane.
- Attach bench supplies with current monitor/limiters to provide +5.0V, +5.5V digital, and +/-5.4V, +12V analog. Set the current limiters to:
 1. +5.0V digital, 400mA
 2. +5.5V digital, 50mA
 3. +5.4V analog, 50mA
 4. -5.4V analog, 50mA
 5. +12.5V analog, 50mA
 6. -12.5V analog, 50mA

Do not connect analog and digital ground (they are connected on the DCB).

- Attach the PROM emulator to the DCB socket (check polarity on silk screen matches emulator socket). Power-on emulator and load test software, configured to run test TEST_WATCHDOG (test #0, ID 10h).
- _____ Attach the spacecraft simulator to the DCB via a break-out box. Power-on S/C simulator and verify 1Hz LED is flashing.
- _____ Start scgse3c.exe. Verify RS232->IDPU LED Flashes 1/second.

OK: _____

5.2. Power-up

- Turn all the power supplies on simultaneously. Turn off immediately if any supply hits its current limit.
- Measure the current dissipation on each supply:
 1. +5.0V digital: _____ mA
 2. +5.5V digital: _____ mA
 3. +5.4V analog: _____ mA
 4. -5.4V analog: _____ mA
 5. +12.5V analog: _____ mA
 6. -12.5V analog: _____ mA

5.3. Verify Stable Oscillator Operation

- Using an oscilloscope verify that the output of the oscillator generates a clean periodic clock. Probe at IDPU-J1 pin 9 (HRECCLK+, which should be 5.0MHz 0-5V square wave; Nominal = 1V-3V, 4ns rise/fall time, <2Vpp ringing) (SGND is on IDPU-J1 pin 33). Heat and cool the BCF FPGA with a heat gun / freeze spray from around 0C (frost starts to form) to about +50C (hot

to the touch) and verify continuing clock operation. Verify clock operation from power-up both warm and cold.

OK: _____

5.4. **Install DCB Test Board**

- Power-off DCB
- Attach DCB test board to IDPU-J6
- Power-on DCB
- Verify 1Hz LED is flashing on test board
- Push Reset button on DCB test board. Verify Reset LED Flashes and data LEDS light is sequence (test code startup)

OK: _____

Measure the +5.0V digital supply current: _____

5.5. **Measure Power-on Reset**

With a storage digital oscilloscope measure the power-on reset time on the DCB backplane (pin C10). Measure the time from +5.0VD crossing 4V to RESET going inactive. _____

If available, repeat with ETU PCB and LVPS:

+5.0VD (backplane pin A18) to RESET inactive: _____

+5.5VD (backplane pin B19) to RESET inactive: _____

6. **Verify DCB Processor and its Interfaces**

The following tests run a sequence of test programs on the flight processor to verify correct operation of the DCB. Configure test.a to start on test zero and download to the ROM emulator. The code will start on the first test (test #0) on reset (push Reset button on the DCB test board). Subsequent tests can be accessed by pushing the Trap button on the DCB test board with the SID switch in the + position, with the test number incrementing by one each time Trap is pushed. Putting the SID switch in the 0 position and pushing the Trap button will decrement the test number.

Each test is preceded by a display on the diagnostic LEDs indicating which test is being run. Verify the correct test number on the LEDs for each test below.

Unless otherwise stated, run scgse3c.exe on the spacecraft simulator gse.

6.1. **Watchdog Timer (LED=10h)**

This test checks the watchdog timer by not resetting the timer and letting it reset the processor. The LEDs should show the test number and then increment briefly (about 2-3 seconds) at high rate until the watchdog timer fires causing a reset and a repeat of the sequence.

OK: _____

The PROM power is not used by the ROM emulator. To verify that the PROM power switch functions, measure the voltage on pin 24 of the PROM (should be 5.0V+/-0.4V)
PROM Voltage: _____

Power off and back on. Verify that the power-on reset correctly resets the system back to test 0.

OK: _____

6.2. **PROM to RAM (LED=20h)**

This test copies the PROM code image to the RAM, and then executes out of the RAM. This verifies that the processor can execute out of both PROM and RAM. If the code works properly, the LEDs should increment at about 100Hz.

OK: _____

The PROM power should now be off. Measure the voltage on pin 24 of the PROM (should be 0V) PROM Voltage: _____

Verify that reset on the DCB test board causes the processor to reset back to test 0:

OK: _____

TRAP back to PROM test (LED=20h). Verify that Reset on the spacecraft simulator GSE causes the processor to reset back to Watchdog test (LED = 10h):

OK: _____

6.3. **RAM Test #1 (LED = 21h)**

This test does not do much. Verify that the LEDs decrement.

OK: _____

6.4. **RAM Test #2 (LED = 22h)**

This test writes a pattern to the memory and then reads it back and compares. The LEDs should increment through with the address, then show success (AAh) or failure (Error code alternating with 00h).

OK: _____

6.5. **Timer Interrupt Test (LED = 30h)**

This test sets the timer interrupt rate to 256Hz, and then counts interrupts on the LEDs. The LEDs should count at 256Hz.

OK: _____

6.6. **1Hz Clock Test (LED = 31h)**

This test counts 1Hz interrupts on the LEDs.

OK: _____

6.7. Clock Register Test (LED = 32h)

This test reads back the clock register once a second (on the 1Hz interrupt) and outputs the LSByte to the LEDs. It also sends the 4-byte time register to the spacecraft GSE, LSByte first (note that the GSE display updates every 16 bytes received). The clock is preset to the value 112233FF hex.

OK: _____

6.8. Clock Roll-over Test (LED = 33h)

This test verifies all the bit transitions of the seconds clock counter by presetting the clock to the value just before a bit transitions, waiting for the 1Hz tick, and the verifying the new value (for example 007FFFFFFF -> 00800000). Spacecraft GSE will show the starting point of each roll-over test as it happens, while the LEDs will show the test number (1-32). After checking each of the 32 bits, a success code is displayed (AAh).

OK: _____

6.9. Clock Sub-seconds Test (LED = 34h)

This test checks the action of the sub-seconds counter by displaying it on the LEDs. The LEDs should count at 256Hz.

OK: _____

6.10. Telemetry Test #1 (LED = 41h)

This test checks the Telemetry DMA channel. It generates a series of 4-byte telemetry blocks consisting of A0h, A1h, A2h, and a counter that increments once a block. These are sent once a second (asynchronously). The LEDs should show the counter value, incrementing once a second, and the spacecraft GSE should show the 4-byte telemetry.

OK: _____

6.11. Telemetry Test #2 (LED = 42h)

This test is similar to the previous one, except a full 1466-byte telemetry packet is generated. The pattern should consist of:

A5 F0 01 02 01 02 01 02 01 02 01 02 01 02 01 02 01 02 01 02

01 02 cc cc cc cc xx xx xx xx xx xx xx xx xx xx

...

AA

The cc values are replaced by the clock register LSB first (increments once a second, starting at C4C3C2C1h), and the xx values are junk. Note that the last byte should be AAh. GSE version scgse5e.exe is better for displaying this data.

OK: _____

6.12. Command Test #1 (LED = 48h)

This test runs both command and telemetry DMA channels. The telemetry data should be the same as Telemetry Test #1. The first byte of each command should be displayed

on the LEDs once a second (asynchronously). The spacecraft GSE sends a counter incrementing at 1Hz in the first command byte, which is what will appear on the LEDs.

OK: _____

6.13. **Command Echo Test (LED = 49h)**

This test is similar to the above test except that it runs synchronously to the 1Hz interrupt, and it echos in the telemetry channel the data it receives in the command channel. This is a 1-second counter in the first byte, followed by 3 bytes of the command received in the last second. The LEDs will show the DMA IRQ count, which should increment by 2 each second. Send a command (the command bytes go into the status field on the GSE). Verify that the command appears in the telemetry.

OK: _____

6.14. **ADC Power Test (LED = 50h)**

This test cycles the ADC 'Nap mode' switch on and off periodically (1 second on, 1 second off). Nap mode reduces the power requirements of the ADC on the +/-5V analog supplies. Measure the current on these supplies in each state:

1. +5.4V analog ADC ON: _____ mA
2. -5.4V analog ADC ON: _____ mA
3. +5.4V analog ADC NAP: _____ mA
4. -5.4V analog ADC NAP: _____ mA

6.15. **ADC Large Signal Test (LED = 51h)**

This test puts the 8 MSBs of the converted value of the analog housekeeping onto the LEDs. Insert a DC supply into the analog housekeeping pin on the backplane with the following voltages on it and record the reading on the LEDs:

1. -2.40V: _____
2. -1.00V: _____
3. 0.0V: _____
4. +1.00V: _____
5. +2.40V: _____

6.16. **ADC Small Signal Test (LED = 52h)**

This test is similar to the previous, except the 8LSBs of the ADC value are displayed. Ground the analog housekeeping pin on the backplane to signal ground and measure the range of values seen on the LEDs (noise level): _____

Now verify that the over-current trip on the ADC works. Connect a 33 ohm resistor from signal ground on the backplane, and momentarily connect to the case of Q3. This cause the over-current detect to shut off the ADC power. Measure the voltage on the case of Q3: _____ V

Re-run the previous test by setting SID to 0 and pushing TRAP on the DCB test card (back to LED=51h). This should reset the current trip. Measure the voltage on the case of Q3: _____ V

6.17. Particle Detector Test A (LED = 60h)

This test displays the value of the particle detector A counter on the LED. This counter is accumulated for 1/8 second and log-compressed. The A counter threshold is set by the threshold DAC, which has been set to 64 in this test. Attach a tail-pulse generator with positive polarity, short rise time (20ns), and 10us fall time. Set a rate around 1KHz, and adjust the amplitude until just at the threshold (counts at 50% of full rate). Measure the pulse height on an oscilloscope:

PDA Threshold = _____mV @ threshold = 64.

Increase the pulse amplitude by about a factor of 2. Record the counts on the LED at the following input rates:

10Hz: _____ (expect 01-02h)
 100Hz: _____ (expect 0C-0Dh)
 1KHz: _____ (expect 3F-40h)
 10KHz: _____ (expect 73-74h)
 100KHz: _____ (expect A8-A9h)

6.18. Particle Detector Test B (LED = 61h)

This test is the same as the previous except that the B counter is displayed on the LED. The B counter threshold is fixed, and should be about twice what was measured for the A-counter. Set a rate around 1KHz, and adjust the amplitude until just at the threshold (counts at 50% of full rate). Measure the pulse height on an oscilloscope:

PDB Threshold = _____mV

Increase the pulse amplitude by about a factor of 2. Record the counts on the LED at the following input rates:

10Hz: _____ (expect 01-02h)
 100Hz: _____ (expect 0C-0Dh)
 1KHz: _____ (expect 3F-40h)
 10KHz: _____ (expect 73-74h)
 100KHz: _____ (expect A8-A9h)

6.19. Particle Detector DAC Test (LED = 62h)

This test checks the particle detector B-counter threshold DAC. The DAC is ramped linearly over its range at about 4Hz. The LED displays the B counter value. Set the pulser to 10KHz. Record the count rate at the following pulser amplitudes:

64mV: _____
 32mV: _____
 16mV: _____
 8mV: _____
 4mV: _____

6.20. Safe Test (LED - 70h)

This test verifies the SAFE signal from the spacecraft gets correctly reported to the processor. The SAFE bit is displayed on the LEDs. Verify that the LED responds to the SAFE button on the GSE (it stays lit about 1 second after the button is pushed).

OK: _____

6.21. Miscellaneous Status Bits Test (LED = 71h)

This test verifies a number of programmable bits in the system can be set and read back. If correct, it will display the success code on the LEDs (AAh).

OK: _____

6.22. DIF Test (LED = 80h)

This test verifies the ability of the DCB to access registers on the DIF across the backplane. It sets bits in the DIF and then reads them back and checks. To perform this test, a DIF test card or DIB ETU must be installed into the VME rack. It should be addressed as DIB board number zero. If correct, it will display the success code on the LEDs (AAh).

OK: _____

Measure the power with the ETU DIB installed (AFE is OFF):

1. +5.0V digital: _____ mA
2. +5.5V digital: _____ mA
3. +5.4V analog: _____ mA
4. -5.4V analog: _____ mA
5. +12.5V analog: _____ mA
6. -12.5V analog: _____ mA

7. Verify High Speed Telemetry Throughput

This test requires the ADP and DIB ETUs be installed in the chassis. No input connections need be made to the ADP, but a tail pulser needs to be attached to the DIB front segment input and adjusted for 10KHz positive going tail-pulses with 100us fall times and 20ns rise time. Start up scgse5e.exe and ssr.exe. Enable and power on the DIB and ADP. Configure the ADP to generate its test pattern (ramp). Enable telemetry from both the ADP (10) and DIB (1), plus monitor rates (12) and fast rates (11). Set the SSR GSE to 1Mbyte buffer Size.

Increase the current limits to:

1. +5.0V digital, 500mA
2. +5.5V digital, 700mA
3. +5.4V analog, 100mA
4. -5.4V analog, 100mA
5. +12.5V analog, 100mA
6. -12.5V analog, 100mA

With the system running, measure the current:

- 1. +5.0V digital: _____ mA
- 2. +5.5V digital: _____ mA
- 3. +5.4V analog: _____ mA
- 4. -5.4V analog: _____ mA
- 5. +12.5V analog: _____ mA
- 6. -12.5V analog: _____ mA

On the SSR display, select monitor rates and record the rates for DIB 0:

	Front Segment	Rear Segment
Reset	_____	_____
Slow Valid	_____	_____
Slow>ULD	_____	_____
Fast Valid	_____	_____
Live Time	_____	_____

Accumulate for a 10 second interval. Record the packet statistics:

- Kbytes: _____
- Lost Sync: _____
- Total Packets: _____
- Event Packets: _____
- Fast Rates: _____
- Mon. Rates: _____
- ADP Science: _____
- ADP Diag.: _____
- Other Packets: _____

Display Event Statistics. Verify that only front detector 1 events are recorded

OK: _____

Display Spectra. Verify that events are tightly bunched with no random energy events.

OK: _____

Display raw data from Fast rates. Record detector 1 counts: _____

Save a block of data for 10 seconds. Post-process it with ADPDCBRamp.exe. Record the statistics:

- Packet Checked: _____
- Lost Sync: _____
- Discontinuities: _____
- Single Word Errors: _____
- Ramp Length Errors: _____

8. Verify Interface Signal Characteristics

8.1. *Spacecraft Interface (IDPU-J1)*

- Start Command test program on the DCB (LED=48h). Start SSR and scgse5e on the spacecraft GSE.
- Use an oscilloscope to verify that the following signal characteristics. All signals should be digital 0-4volts, with rise/fall times < 20ns and < +/-1V ringing. SGND is on pin 33.
 1. ___ Pins 1-8, HRECDAT0+...HRECDAT7+ active
 2. ___ Pins 20-27, HRECDAT0-...HRECDAT7- active
 3. ___ Pin 9 and 28, HRECCLK+ and HRECCLK-, active, 5MHz, opposite phase (note typical voltage seen is 1V-3V)
 4. ___ Pins 10 and 29, HRECVLF+ and HRECVLF-, active, opposite phase
 5. ___ Pins 13 and 32, Telemetry+ and Telemetry-, active, opposite phase
- Measure impedance between the following signals that run through the DCB with the DCB power off and the spacecraft simulation GSE disconnected:
 - TMP: IDPU-J1 pin 19 and Backplane pin B26: _____
 - TMPRET: IDPU-J1 pin 37 and Backplanbe pin C26: _____
 - RASTMP: IDPU-J1 pin 18 and Backplane pin B25: _____
 - RASTMPRET: IDPU-J1 pin 36 and backplane pin C25: _____
 - TMP: IDPU-J1 pin 19 and power supply ground: _____
 - TMPRET: IDPU-J1 pin 37 and supply power ground: _____
 - RASTMP: IDPU-J1 pin 18 and power supply ground: _____
 - RASTMPRET: IDPU-J1 pin 36 and power supply gnd: _____

8.2. *Backplane Interface (P1)*

- Disconnect power and measure the impedance between analog power supply ground and digital power supply ground: _____
- Use an oscilloscope to verify that the following signal characteristics. All signals should be digital 0-5volts, with rise/fall times < 20ns:
 1. ___ ADDR0-7 on A1-A8 active
 2. ___ DATA0-7 on B1-B8 active
 3. ___ DATA8-15 on C1-C8 inactive
 4. ___ BUSCLK on A10 10MHz
 5. ___ RD (B10), PRD (B11), BUSCLK (A10) timing per HSI_SYS_019. Measure time from BUSCLK to RD (TCTRL): _____ ns
 6. ___ CLK1M on A16 1MHz, 100ns pulse
 7. ___ CLK1HZ on B16 1Hz, 100ns pulse

8.3. Particle Detector Interface (IDPU-J5)

- Measure +5.4V on IDPU-J5 pin 1: _____
 - Repeat with 470 ohm to pin 2: _____
- Measure -5.4V on IDPU-J5 pin 3: _____
 - Repeat with 470 ohm to pin 2: _____
- Measure SGND on IDPU-J5 pin 2: _____
- Measure impedance between analog power supply ground and SGND on IDPU-J5 pin 2: _____
- Measure impedance between analog power supply ground and SGND on IDPU-J5 coax shield: _____
- Measure impedance between analog power supply ground and Thermistor signal on IDPU-J5 pin 4: _____
- Measure impedance between Thermistor signal on IDPU-J5 pin 4 and backplane pin A25: _____