

HESSI RAS/SAS Simulator Description
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The RAS/SAS Simulator (RSS) connects to the HESSI IDPU ADP and simulates the operation of RAS or SAS by sending images to the ADP. Within the RSS these images come not from a CCD and A/D converter but from an image memory.

IMAGE MEMORY DESCRIPTION

Two 27C080 OTP EPROMs in the RSS form the image memory of 1024K 16-bit words. One image consists of 2048 video pixels. The RSS memory stores one pixel per word, so it can hold up to 512 images of 2048 pixels each.

A RAS or SAS pixel is derived from a 12-bit A/D converter. RAS/SAS logic reduces this to a 10-bit value for transmission to the ADP. RSS reads the low 10 bits of an RSS memory word and transmits it as the 10-bit pixel value. The high six memory bits control the sequence of images.

RSS Memory Address:

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
-----										*-----*									
Index to Image 0-511										Index to Word 0-2047 of one Image									

RSS Memory Word Contents:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----						*-----*									
6 Control Bits						10-bit Pixel									

The RSS reads the first 2048 (0800h) words of the first image sequentially from memory starting at address 00000h. It reads the 2048 words of the next image from sequentially higher address, continuing in this way until it reaches the last word of the 512th image (address FFFFFh). Then it returns to address 00000h.

By using the control bits in the scheme described below, RSS can send an arbitrary sequence of images from its memory and repeat one image an arbitrary number of times.

A 12-bit control word is built from the control bits of the last two memory words of a 2048-word image as follows:

Word No. (0-2047)	D15	D14	D13	D12	D11	D10
2046	n	n	n	n	n	n
2047	c1	c0	m	m	m	m

The high two bits (c1,c0) are a command, and the low ten bits (m,n) are a value used by the command.

c1 c0 Command

1	1	NOP (continue at next address for next image)
1	0	Repeat this image mmmmmnnnnnn (0-3FFh, 0-1023d) more times
0	1	Go to image mmmmmnnnnnn (0-1FFh, 0-511d) next
0	0	(Reserved)

RSS ignores the high six bits of words 0-2045 of each image. (I recommend setting these bits to 1, so that they will not be mistaken for commands, and because EPROM will usually program faster if unused bits are 1.)

Bits D15-D8 (the MS byte) are in PROM U5; bits D7-D0 (the LS byte) are in PROM U4.

READOUT TIMING

The first bit of the serial data stream from the RSS becomes valid 200-250 nanoseconds after the rising edge of the start pulse; the data then continues for 2087 microseconds (one image).

SPIN SYNCHRONIZATION

A rising edge on the SPIN SYNC IN connector (J3) will cause the RSS to start reading from memory address 00000h when the next start pulse arrives from the ADP.

CONNECTORS

J1 - Data (same as RAS & SAS)
J2 - Power (same as RAS & SAS)
J3 - Spin Sync In. BNC. Rising TTL edge causes readout to start from beginning of memory at next start pulse.

LEDs

+14.5V, +12V, +5VD, +5VA, -5V - On when corresponding power service is on at J2. Each draws about 9 milliamps.

TEST2, TEST1 - Blinks when test LED is activated.

SPIN SYNC - Blinks when rising edge arrives at SPIN SYNC IN connector.

START - Blinks at start of image readout (STRT from ADP).

RDOUT CLK - Blinks when RSS is clocking out readout data (CLK to ADP).

FSR - Blinks when RSS is clocking out readout data (FSR to ADP).

A, B - (spares).

MODE2, MODE1, MODE0 - Show state of M2, M1, M0 signals from ADP.

SWITCHES

RESET - Resets RSS logic as at power on. (In addition RSS has an internal R-C power-on reset lasting about 100 milliseconds.)

RUN/STOP - RUN = Normal operation; STOP = ignore start and sync signals (don't do readout).

SAS/RAS - (spare).

IMAGE - (spare).

E - (spare).

OPT2, OPT1, OPT0 - Same as jumpers on SAS.

POWER CONSUMPTION

Load resistors in the RSS cause it to draw the following approximate power supply currents

	<u>RAS</u>	<u>SAS</u>
+14.5V:	16 mA	12 mA
+12V:	50 mA	14 mA
+5VD:	134 mA	134 mA
+5VA:	44 mA	40 mA

PROMs

Two 27C080 OTP EPROM, 120 ns or faster, PLCC-32 package, Atmel AT27C080-12JC or equivalent.

REVISIONS

B 1999-07-30

C 2000-09-21 Delete IMAGE switch; double EPROM; add load resistors.