HESSI IDPU Backplane Signals

Dave Curtis 1999-Apr-13

1. Overview

The HESSI IDPU backplane will be used to transfer data between the nine detector interface boards, the Aspect Data Processor (ADP) board, the Power Controller Board, and the Data Controller board, plus provide power to all boards. Data will be transferred over a common digital data bus. The Data Controller board includes a processor and packet formatter both connected to the bus via a Bus Controller. The Bus Controller arbitrates bus usage, performing processor transfers on request, periodic transfers to the packet formatter, Event transfers to the packet formatter on request from the Detector Interface boards, and Aspect packet data to the packet formatter on request by the ADP. Data to be transferred includes:

1. Control information from the Data Controller board (processor) to the Detector Interface, ADP, and Power Controller boards
2. Digital Status and Monitor Rates data from the Detector Interface, ADP, and Power Controller boards to the Data Controller board (processor)
3. Event data from the Detector Interface boards to the Data Controller board (packet formatter) on request by the Detector Interface boards
4. Fast Rates data from the Detector Interface boards to the Data Controller board (packet formatter) periodically when enabled.
5. Monitor Rates data from the Detector Interface boards to the Data Controller board (packet formatter) periodically
6. Aspect Packet data from the ADP to the Data Controller board (packet formatter) on request by the ADP.

In addition, timing information is provided from the Data Controller board in the form of timing pulses (1MHz and 1Hz). This is used by the ADP and Detector Interface boards to generate time stamps on events.

There is also an analog bus for the transfer of analog housekeeping to the ADC on the Controller board. This is a single line shared by all nine detector interface boards, the ADP board, and the Power Controller board. The processor selects which of the boards is enabled onto the analog line by command over the data bus.

2. Data Bus

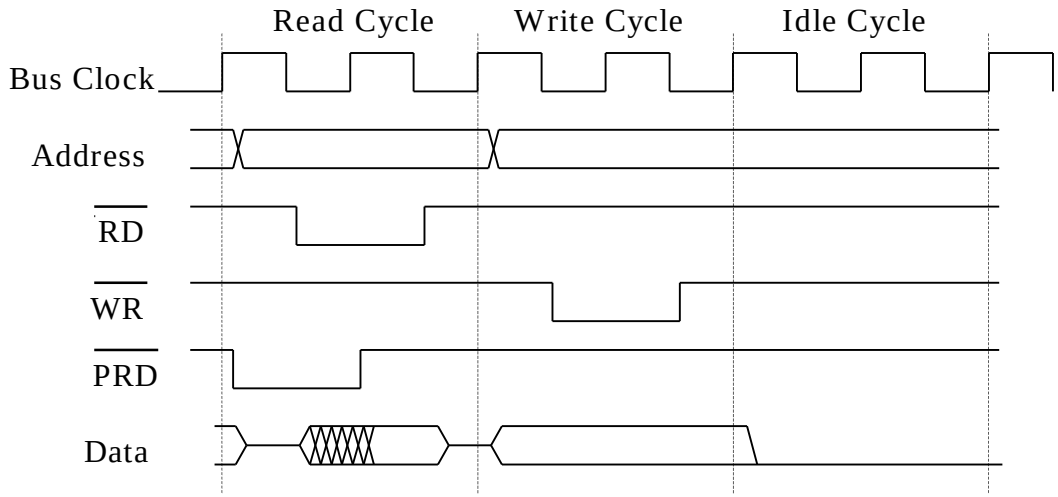
The data bus consists of an 16 bit bidirectional data path, an 8 bit address, and read and write control signals. The 4 MSB of the address select which board is the destination of the current transfer; codes 0-8 select one of the Detector Interface Boards, code 9 selects the Aspect Data Processor, code 10 selects the Power Controller board, and 11-14 are reserved for use on the Controller board. Code 15 is used for special broadcast commands to all boards, such as the time

code. The 4 LSB of the address select one of up to 16 16-bit registers on the selected board to be read or written to.

Bus Address 4 MSB decoding

Value (Hex)	Board Selected
0	Detector Interface Board #0
1	Detector Interface Board #1
2	Detector Interface Board #2
3	Detector Interface Board #3
4	Detector Interface Board #4
5	Detector Interface Board #5
6	Detector Interface Board #6
7	Detector Interface Board #7
8	Detector Interface Board #8
9	ADP
A	Power Controller
B	None
C	None
D	None
E	None
F	Broadcast (All)

Read and Write control signals will determine data bus direction and timing. When the bus is idle, the data bus controller will drive so that it does not remain in a high-impedance state for very long. Bus timing will be arbitrated by the data bus controller on the Controller board, based on a 10MHz bus clock.



Bus Timing Diagram

Bus Timing (TBR)

Symbol	Parameter	MIN	MAX
Taddress	Bus Clock rising edge to Address	0	25ns
Tctrl	Bus Clock falling edge to Control line change (RD, WR)	0	25ns
Twrdata	Bus Clock rising edge to Data on Write Cycle (or high impedance on Read Cycle)	0	25ns
Tdatasetup	Read Cycle Data Setup Time requirement (from RD rising edge)	25ns	
Tdatahold	Read Cycle Data Hold Time requirement (from RD rising edge)	10ns	

2.1. *Transfer Requests*

Each detector interface board shall provide an Event Transfer Request (ETR) signal to the Data Controller board to indicate it has an event to be collected. In addition, the ADP shall generate an ETR signal when it has packet data to be collected. These ten signals are used by the data bus controller to arbitrate bus usage. The Event Transfer Request should remain active until the 2 16-bit words of the event have been read out by the data bus controller (from address X0 and X1 hex, in that order, for Detector Interface board number X). For the ADP, the ETR shall remain active until the data packets(s) have been completely read out.

In addition, the ADP needs a signal to synchronize the start of a packet. The Start of Packet (SOP) signal shall go high immediately after the Data Controller has read out the last data word of a packet (on the rising edge of RD), and shall remain high until the first word of the next packet is being read (on the rising edge of RD). The data bus controller shall read Packet data from register 1 (address 91 hex) of the ADP in response to its ETR.

2.2. *Register Addressing*

A jumper on each Detector Interface board tells the board which board number it is, so it knows which addresses to respond to and which Event Transfer Request line to activate. ADP and Power Controller boards have their decoding hard-wired.

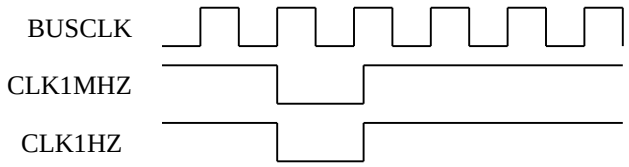
Register address codings and meanings for the Detector Interface boards are documented in HSI_IDPU_010, for the ADP in document HSI_IDPU_013, and for the Power Controller in document HSI_IDPU_008.

Broadcast command addresses for Write transfers

Address (Hex)	Contents
F0	Analog Housekeeping Select
F1	Unused
F2	Unused
F3	Unused
F4	unused
F5	unused
F6	unused
F7	unused
F8	unused
F9	unused
FA	unused
FB	unused
FC	unused
FD	unused
FE	Time Code Word 0 (MSB)
FF	Time Code Word 1 (LSB)

3. Timing

The backplane provides two timing pulses; CLK1MHZ, and CLK1HZ. These clocks are based on the stable spacecraft clock, and should be used for generating time tags and for synchronous data collection. CLK1MHZ is a 2^{20} Hz clock (1,048,576 Hz), and CLK1Hz is a 1Hz clock. These clocks are synchronous; there are always 2^{20} CLK1MHZ clocks per CLK1HZ clock pulse. The timing of these clocks is shown below. The clock edges are synchronized to the BUSCLK rising edge to simplify state machines in the detector interface boards (at the cost of 100ns jitter).



Clock Timing

The Data Controller board will broadcast the time at the most recent 1Hz time tic once a second by writing to registers FEh and FFh. This time code will be spacecraft time, the number of seconds since a TBD epoch. The time value sent is 32 bits of integer seconds; the fractional seconds are zero at the time of the CLK1HZ pulse. A time couter can be implemented using a 20 bit counter clocked by CLK1MHZ falling edge and reset by CLK1HZ, and 1 32 bit counter clocked by CLK1HZ falling edge, and asynchronously loaded when the time words are written.

4. Analog Housekeeping

Each board that provides analog housekeeping onto the shared housekeeping bus decodes analog housekeeping select. The 4 MSB of the select value sent indicates which of the boards should provide a value onto the analog housekeeping line. The other boards should set their connection to the analog housekeeping line to a high impedance state. The 4 LSB of the select value indicates which value the selected board should put onto the analog housekeeping line. Typically the select value 4 MSB are decoded with the board number to run the enable of an analog multiplexer (such as a Harris 508ARH), while the 4 LSB go to the multiplexer select. The following table indicates how the decoding of the 4 MSB of the select signals. The coding of the 4 LSB are described in document HSI_IDPU_010 for the detector interface boards, document HSI_IDPU_013 for the ADP, and document HSI_IDPU_008 for the Power Controller board.

Analog data sampling accuracy is limited by source impedance due to bus bias currents, bus capacitance settling time, and noise pick-up. A source impedance of < 50kOhms should result in a measurement good to 1%, while a low impedance source measured through a 508ARH multiplexer should be good to 0.1%. The analog bus shall be routed to minimize noise pick-up.

Analog Housekeeping Select 4 MSB decoding

Value (Hex)	Board Selected
0	Detector Interface Board #0
1	Detector Interface Board #1
2	Detector Interface Board #2
3	Detector Interface Board #3
4	Detector Interface Board #4
5	Detector Interface Board #5

6	Detector Interface Board #6
7	Detector Interface Board #7
8	Detector Interface Board #8
9	ADP
A	ADP
B	Unused
C	Power Controller
D	Power Controller
E	Power Controller
F	Power Controller

5. Physical Interface

The IDPU is housed in a 6U VME chassis, with a 3U VME backplane in the J1 connector location. The backplane is physically an unterminated VME backplane, but the VME standard is not used for the signal definitions.

NOTE: a trailing '/' in a signal name indicates an active-low signal.

Backplane Connector J1 Pinout

Pin #	Signal Name	Signal Function
A1	ADDR0	Address Bit 0 (LSB)
A2	ADDR1	
A3	ADDR2	
A4	ADDR3	
A5	ADDR4	
A6	ADDR5	
A7	ADDR6	
A8	ADDR7	Address Bit # 7 (MSB)
B1	DATA0	Data Bit #0 (LSB)
B2	DATA1	
B3	DATA2	
B4	DATA3	
B5	DATA4	
B6	DATA5	
B7	DATA6	
B8	DATA7	
C1	DATA8	
C2	DATA9	
C3	DATA10	
C4	DATA11	
C5	DATA12	
C6	DATA13	

C7	DATA14	
C8	DATA15	Data Bit #15 (MSB)
A9	DGND	Digital Ground
B9	WR/	Bus Write Strobe
C9	DGND	Digital Ground
A10	BUSCLK	Bus Clock
B10	RD/	Bus Read Strobe
C10	RESET/	System Reset
A11	DGND	
B11	PRD/	Pre-Read Strobe
C11	ETR0	Event Transfer Request for Detector Interface Board #0
A12	ETR1	
B12	ETR2	
C12	ETR3	
A13	ETR4	
B13	ETR5	
C13	ETR6	
A14	ETR7	
B14	ETR8	
A15	DGND	Digital Ground
B15	ADPTR	ADP Transfer Request
C15	ADPSOP	ADP Start Of Packet
A16	CLK1MHZ	1MHZ timing Clock
B16	CLK1HZ	1HZ timing Clock
C16		
A17	DGND	Digital Ground
B17		
C17		
A18	VP5D	+5V Digital (Regulated)
B18	VP5D	+5V Digital (Regulated)
C18	VP5D	+5V Digital (Regulated)
A19	DGND	Digital Ground
B19	VP5DU	+5V Digital Unregulated (5.4V -0/+10%)
C19	VP5DU	+5V Digital Unregulated (5.4V -0/+10%)
A20		
B20	DGND	Digital Ground
C20		
A21	VHTR	IDPU Heater +28V
B21	VHTR	IDPU Heater +28V
C21	VHTR	IDPU Heater +28V
A22	VHTRRET	IDPU Heater +28V Return
B22	VHTRRET	IDPU Heater +28V Return
C22	VHTRRET	IDPU Heater +28V Return
A23		

B23	DGND	Digital Ground
C23		
A24	VP15	+15V
B24	VP15	+15V
C24	VP15	+15V
A25	PDTMP	Particle Detector Thermistor (returned to SGND)
B25	RASTMP	RAS Temperature Sensor (to Spacecraft)
C25	RASTMPRET	RAS Temperature Sensor Return (to Spacecraft)
A26	AHKP	Analog Housekeeping Signal
B26	TMP	IDPU Temperature Sensor
C26	TMPRET	IDPU Temperature Sensor Return
A27	VP12	+12V
B27	VP12	+12V
C27	VP12	+12V
A28	VP5	+5V
B28	VP5	+5V
C28	VP5	+5V
A29	VM5	-5V
B29	VM5	-5V
C29	VM5	-5V
A30	VM12	-12V
B30	VM12	-12V
C30	VM12	-12V
A31	AGND	Analog Ground
B31	AGND	Analog Ground
C31	AGND	Analog Ground
A32	AGND	Analog Ground
B32	AGND	Analog Ground
C32	AGND	Analog Ground

5.1. *Backplane*

The J1 pinout differs from the VME standard, but is compatible with a standard passive VME backplane (so commercial VME backplanes can be used for testing purposes with some modifications). For the flight backplane, there shall be a ground layer broken into two parts with the gap around the 24th row of pins. The top half of the ground plane shall be DGND, and the bottom half shall be AGND. There shall be provision for optional soldered-in wire jumpers between the ground planes located at every second J1 connector. VP5D, VP5, VM5, VP12, VM12, VP15, VHTR, and VHTRRET should be carried on heavy > 0.1" wide traces. All remaining pins shall be bussed individually (including currently unused pins). VHTR, VHTRRET, TMP, and TMPRET shall be connected to pads to allow them to be wired to components attached to the IDPU chassis. AHKP shall be routed away from all signals except AGND to avoid crosstalk (surround the signal with AGND). No bypassing or termination components shall be on the backplane. PDTMP, RASTMP, and RASTMPRET signals are routed from the Data Controller Card to the Power Controller Card over the backplane.