HESSI IDPU Processor Specification
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1. Introduction

This document is a preliminary specification for the IDPU processor system. The processor controls the HESSI instruments, collects, monitors, and formats instrument State of Health (SOH) data, and communicates with the spacecraft over a serial interface. The processor is part of the Data Controller Board, along with the Bus Controller FPGA (BCF), Packet Formatter FPGA (PFF), an Analog to Digital Converter for measuring housekeeping values, and a Particle Detector Interface. In addition to configuration registers on the BCF and PFF, the processor can access registers in other boards in the IDPU VME chassis over the IDPU backplane via the BCF.

The processor does not directly interact with science telemetry – this is handled automatically by the FPGAs. The processor can control the flow of data via various control registers. The processor does collect and format SOH and diagnostic data.

1.1 Related Documents

These documents are available on the web at:

ftp://apollo.ssl.berkeley.edu/pub/hessi/

[1] HESSI IDPU Backplane Signals (HSI_SYS_019B)
[2] HESSI IDPU Bus Controller FPGA Specification (HSI_IDPU_004A)
[3] HESSI IDPU Packet Formatter FPGA Specification (HSI_IDPU_005A)
[4] HESSI IDPU to Spacecraft ICD (HSI_SYS_001A)

2. Core Processor System

The core processor system consists of a microprocessor, DMA chip, memory, and glue logic. Interface to the rest of the system shall be through I/O registers, as described in section 3.

2.1. *Processor/DMA*

The processor shall use a Harris 80C85RH microprocessor. It shall run at 3.333MHz (X1 input) using a clock provided by the BCF (BUSCLK/3). A Harris 82C37ARH DMA chip, also running at 3.333MHz, shall be used to service the spacecraft serial interface (see Section 3.1). The DMA chip shall be connected to the processor using the HOLD/HLDA bus access handshaking signals. See the DMA chip data sheet on recommended interfacing.

2.2. *Memory*

The processor shall have an 8Kbyte PROM (Raytheon R29793) and a 32Kbyte static RAM (UTMC UT7156C-40). The PROM shall have a FET power switch to allow it to be turned off (when powered off, the selected PROM does not require bus isolation – it will not adversely effect the processor bus). Both the PROM and the RAM shall be addressed stating at zero in the address space. When the PROM is powered on, read accesses to the first 8Kbytes will be directed to the PROM, while all writes and reads above 8Kbytes will be directed to the RAM. When the PROM is powered off, all memory accesses will be directed to the RAM. On reset, the PROM will be set to the powered-on state, but can be powered on or off later via an I/O register.

2.3. *Glue Logic*

Glue logic shall be implemented in an FPGA, possibly part of the BCF and/or PFF. Glue logic functions include:

- Clock Generation (see section 2.1)
- Memory Decoding (see section 2.2)
- Address LSB latch using processor ALE signal (see 8085 specification)
- Reset Logic, including a Watch Dog Timer
- Interrupt Logic

2.3.1. Reset Logic / Watchdog Timer

There are 3 sources of processor reset:

- Power-on reset
- Spacecraft reset
- Watchdog Reset

These signals can be logically OR-ed together, and tied to the processor reset. A processor reset also should cause an IDPU backplane reset (via the BCF).

2.3.1.1 Power-On Reset

The power-on reset shall be generated by an R-C circuit tied to a logic pin on the glue logic FPGA, consisting of a 1Mohm resistor tied to +5V and a 0.1µF capacitor tied to ground. A diode to +5V in parallel with the resistor ensures that the signal does not exceed the +5V value during power-down.

2.3.1.2 Spacecraft Reset

The spacecraft shall provide a logic-level pulse that is activated by ground command to reset the processor.

2.3.1.3 Watchdog Reset

The watchdog system is designed to reset the processor in case it 'crashes'. If the processor fails to output the Watchdog value to the Watchdog I/O register periodically, a reset pulse is generated. The processor should write the value once a second. If two seconds pass without the value being written the processor should be reset. This can be implemented by a flip/flop triggered by the CLK1HZ signal, and reset when the specified value is written to the specified I/O port. Generate a reset pulse on the falling edge of the Flip/Flop.

2.3.2. Interrupt Logic

The 8085 has a number of processor interrupt inputs. Only RST5.5, RST6.5, and RST7.5 shall be used. RST5.5 shall provide a 1 second interrupt, RST6.5 shall provide a Timing interrupt, and RST7.5 shall be caused by the DMA EOP signal (at the end of a transfer). The time tics shall be based and synchronized to the stable clock. The Timing interrupt shall be programmable to one of 8Hz, 16Hz, 32Hz, 64Hz, 128Hz, 256Hz, 512Hz, or 1024Hz via an I/O register. Glue logic shall cause the appropriate edge of the specified signal to set a flip/flop connected to the indicated processor RST signal. The processor shall be able to reset these flip/flops individually by writing to an I/O register.

3. Interfaces

The processor shall interface with the rest of the IDPU and spacecraft through I/O registers. The 8085 has 256 I/O registers. Registers 00h-AFh and F0h-FFh are mapped onto the IDPU backplane by the BCF (see references 1 and 2). The remainder can be used to access registers in the BCF, PFF, DMA, ADC, UART and other systems on the Data Controller Board (allocation of these registers is left to the designer). BCF and PFF registers are described in reference 2 and 3. A few I/O registers are required by the Core processor system as described in section 2. The remainder are described below. These I/O registers shall be implemented in an FPGA, possibly part of the PFF and/or BCF FPGA.

3.1. *UART*

The spacecraft serial interface shall by a standard UART as described in reference 4, and implemented in an FPGA (an FPGA implementation of a similar UART is available). The UART shall use two DMA channels; one for serial input and one for serial output. Data shall be transferred in fixed-length blocks in each direction once a second. A parity error in the receive channel shall be latched in a processor I/O register, indicating an error in the block.

3.2. *ADC*

A Liner Technology LTC1604 16-bit ADC shall be used to convert analog housekeeping values. The processor shall be able to read the converted value, start a new conversion, and monitor the status of a conversion via I/O registers. The ADC should not be directly

connected to the processor bus, but via an FPGA to avoid noise. See the ADC data sheet for details on interfacing (available on the Linear Technology web site).

3.3. *Diagnostic Register*

An 8-bit processor I/O register shall be latched and provided on a diagnostic connector on the Data Controller card, along with it's I/O write strobe. This register can be used during software development of the IDPU processor.