This document describes the interface between the Analog Front End (AFE) circuits on the HESSI detector interface boards and the digital electronics.

1. Events
   The AFE shall produce two independent event channels – Front and Rear. Each event channel shall consist of a 13 bit parallel A/D value plus a positive-going logic strobe of TBD duration. The ADC data will be valid on the TBD edge of the strobe. The Rear events shall also include an energy select bit, indicating which energy range was selected for the ADC conversion.

2. Pulses
   The AFE shall provide the following pulses. They shall be positive-going logic pulses of TBD duration.

   Front Preamp Reset
   Front 4µs Shaper Valid Event (between LLD and ULD)
   Front 4µs Shaper over ULD
   Front Delay Line Valid Event (above LLD)
   Front Delay Line LLD – E1
   Front Delay Line E1-E2
   Front Delay Line E2-E3
   Front Delay Line >E3

   Rear Preamp Reset
   Rear 4µs Shaper Valid Events (between LLD and ULD)
   Rear 4µs Shaper over ULD
   Rear Delay Line Valid Event (above LLD)

3. Live Time
   This signal shall provide a live time indicator, independently for Front and Rear detectors. The signal shall be logic zero when the system is not ready for 4µs Shaper events for some reason (conversion, pile-up, preamplifier reset, over ULD event dead-time, etc), and otherwise a logic one.

4. Time-to-Peak
   Time-to-Peak circuitry for the rear segment produces a 4 (TBR)-bit number to be included with the event word. This data must be valid at the time of the event strobe described in section 1.

5. Leakage Current Monitor
   The AFE shall provide an analog level proportional to the detector leakage current, in the range of zero to 5 volts. The digital electronics can also monitor other analog values in a similar way – use of the feature is TBD.
6. **Discriminator Thresholds**

The Front and Rear detector 4µs Shaper LLD discriminators shall be programmable, using analog levels provided to the AFE by the digital electronics. These values shall be programmable from 0 to 5 Volts using an 8 bit DAC. Other DAC outputs for adjustment of the AFE are TBD.

7. **Calibration Pulser**

A logic level enable signal shall be provided to the AFE to turn on/off the calibration pulser. A zero level indicates off, and a one indicates on. In addition, the amplitude of the pulse shall be programmable. The digital electronics shall provide an analog signal to set the pulse amplitude. The value shall be programmable from 0 to 5 Volts using an 8 bit DAC.

8. **High Voltage Control**

The high voltage power supply voltage level shall be programmable. The digital electronics shall provide a control voltage to set the desired level for the supply. The value shall be zero to 5 Volts using an 8 bit DAC.

9. **Power**

The AFE shall be provided +5V, +12V, -12V (TBR) supplies with TBR current levels and ripple levels. In addition, three logic levels will be provided to control solid-state power switches (FETs). One switch shall control a 28V supply to the high voltage power supply. The second shall control switches on power to the Time-to-Peak (TTP) circuitry. The third shall control switches on power to the rest of the AFE (excluding the CSA and HVPS supplies). The AFE will run in three power levels:

<table>
<thead>
<tr>
<th>Mode</th>
<th>Control</th>
<th>CSA</th>
<th>AFE</th>
<th>TTP</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby</td>
<td>00</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>&lt; 1W</td>
</tr>
<tr>
<td>Normal</td>
<td>01</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>&lt; 3.5W</td>
</tr>
<tr>
<td>TTP</td>
<td>11</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>&lt; 4.5W</td>
</tr>
</tbody>
</table>

(Power levels are per board, and include 0.5W CSA plus HVPS dissipation).

The CSA and HVPS supplies shall be unswitched (except for the HVPS 28V supply). The digital electronics shall work off an unswitched +5 Volt supply.