HESSI Decimation Control Specification
HSI_IDPU_020A
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1. Introduction

The HESSI Detector Interface electronics contains controls to digitally decimate the incoming event stream, so that not all events get sent to telemetry (all events still get counted by the monitor and fast rates counters). When the decimator is enabled, only a (programmable) fraction of the events below a (programmable) energy threshold get passed on (all events above the threshold are sent).

The Front segment decimators shall be used by the flight software to control the event rate to avoid exceeding the spacecraft Soild State Recorder (SSR) capacity. The rear segment decimators shall be programmed from the ground to limit the background rate.

The flight software can also modulate the event rate using the mechanical attenuators. This shall be used by a separate piece of the flight software designed to keep the count rate below the saturation level (about 50,000 events/sec). The attenuator control software shall also enable/disable the fast rates telemetry. The attenuator control software shall be documented elsewhere.

2. Decimation Controls

Each of the Detector Interface Boards (DIB) has separate decimation controls for the front and rear segment of each detector. The DIB control is contained in the Detector Interface FPGA (DIF), as described in document HSI_IDPU_010. The relevant controls consist of:

Control	Reg. (*)	Bit (**)	Settings
Front Event Enable	X2	0	0 = disabled, 1 = enabled
Front Decimation Enable	X2	3	0 = disabled, 1 = enabled
Front Decimation Any	X2	4	0 = off, 1 = decimate all energies (independent of reg X3 energy threshold setting)
Front Decimation Count	X3	0-3	Set the fraction of events that are decimated. See section 2.1 below
Front Decimation Energy	X3	4-7	Set the energy threshold below which events are decimated. See section 2.1 below
Rear Event Enable	X4	0	0 = disabled, 1 = enabled
Rear Decimation Enable	X4	3	0 = disabled, 1 = enabled
Rear Decimation Any	X4	4	0 = off, 1 = decimate all energies (independent of reg X3 energy threshold setting)

Rear Decimation Count	X5	0-3	Set the fraction of events that are decimated. See below
Rear Decimation Energy	X5	4-7	Set the energy threshold below which events are decimated. See below

(* - an X in the register number stands for the DIB number, 0-8. Register numbers are hexidecimal)
(** Bits are numbered from LSB=0 to MSB=15)

The decimation logic is based on when the event arrives, and what its energy is. A counter counts microseconds (2^{20} Hz), counting from zero to the Decimation Count. The counter is reset at the 1Hz clock event, so that all decimators are synchronized. All events are enabled when the counter is zero. At other times, only events with energies above the Decimation Energy are enabled. This is summarized in the tables below.

Decimation Count	Fraction of time events below Decimation Energy are enabled
0	100%
1	1/2
2	1/3
3	1/4
4	1/5
5	1/6
6	1/7
7	1/8
8	1/9
9	1/10
10	1/11
11	1/12
12	1/13
13	1/14
14	1/15
15	1/16

Front Decimation Energy	Front Event Energy levels that are decimated (approx. energies)
0	None
1	0000 - 000F (0 - 5keV)
2	0000 - 001F (0 - 10keV)
3	0000 - 002F (0 - 15keV)
4	0000 - 003F (0 - 20keV)
5	0000 - 004F (0 - 25keV)
6	0000 - 005F (0 - 30keV)
7	0000 - 006F (0 - 35keV)

8	0000 - 007F (0 - 40keV)
9	0000 - 008F (0 - 45keV)
10	0000 - 009F (0 - 50keV)
11	0000 - 00AF (0 - 55keV)
12	0000 - 00BF (0 - 60keV)
13	0000 - 00CF (0 - 65keV)
14	0000 - 00DF (0 - 70keV)
15	0000 - 00EF (0 - 75keV)

Rear Decimation Energy	Front Event Energy levels that are decimated (approx. energies)
0	None
1	0000 - 007F (0 - 40keV)
2	0000 - 00FF (0 - 80keV)
3	0000 - 017F (0 - 120keV)
4	0000 - 01FF (0 - 160keV)
5	0000 - 027F (0 - 200keV)
6	0000 - 02FF (0 - 240keV)
7	0000 - 037F (0 - 280keV)
8	0000 - 03FF (0 - 320keV)
9	0000 - 047F (0 - 360keV)
10	0000 - 04FF (0 - 400keV)
11	0000 - 057F (0 - 440keV)
12	0000 - 05FF (0 - 480keV)
13	0000 - 067F (0 - 520keV)
14	0000 - 06FF (0 - 560keV)
15	0000 - 077F (0 - 600keV)

Notes:

- No decimation occurs when the Decimation Enable control is zero.
- Decimation occurs for all energies when the Decimate Any control is on, independent of the Decimation Energy control and event energy.
- When Decimate Any is off, no Rear events are decimated if the rear segment is in the high energy mode (> about 2.7MeV)

The ultimate control is the event enable, which can disable all events. This shall be used only as a last resort.

3. Inputs to the Front Segment Decimation Control Routine

The on-board decimation control software shall use two parameters as input, the remaining SSR memory capacity, and the state of the attenuators. The spacecraft provides the IDPU the remaining capacity of the SSR once a second, in the form of an 8-bit value which runs from 0=empty to 255=Full. The IDPU controls the attenuators, so it at all times knows their state. There are 4 attenuator states, corresponding to in or out for each of the two attenuators, thin and thick. It is important that the decimation control avoid filling the memory past capacity, as this will result in over-writing the oldest data.

4. Front Segment Decimation Control Routine

The decimation control shall be controlled by a look-up table based on the two input parameters (SSR capacity and attenuator state). Memory capacity shall have 9 ranges, which are shown below:

SSR State	SSR Capacity code	SSR Remaining Capacity
0	0 - 127	50% - 100%
1	128 - 154	40% - 50%
2	153 - 179	30% - 40%
3	178 - 205	20% - 30%
4	206 - 230	10% - 20%
5	231 - 243	5% - 10%
6	244 - 250	2% - 5%
7	251 - 243	1% - 2%
8	254 - 255	0% - 1%

SSR State 8 is a special case. In this state all events, fast rates, and aspect data are disabled, and only monitor rates are enabled into the memory. This is an emergency mode that we hope never to get into.

Ignoring state 8, there are 8 SSR States by 4 Attenuator states, for a total of 32 decimation states. The decimation state shall index a table containing the Front Segment Decimation State (register X3) for each of the 9 detectors (9 bytes total). The Front segment decimation enable shall always be set. Once a second, the flight software shall determine the SSR and attenuator state and set the front segment decimators accordingly.

The default table is shown below. In the default table, all 9 detectors have the same decimation. This table shall be programmable.

[This table needs input from Richard Schwartz]

Attenuator State	SSR State	Decimation Count	Decimation Energy
Thin=OUT, Thick=OUT	0 (50-100%)	0 (100%)	0
Thin=IN, Thick=OUT	0	0	0
Thin=OUT, Thick=IN	0	0	0
Thin=IN, Thick=IN	0	0	0
Thin=OUT, Thick=OUT	1 (40-50%)	1 (50%)	4
Thin=IN, Thick=OUT	1	1	5
Thin=OUT, Thick=IN	1	1	6
Thin=IN, Thick=IN	1	1	7

Thin=OUT, Thick=OUT	2 (30-40%)	2 (33%)	4
Thin=IN, Thick=OUT	2	2	5
Thin=OUT, Thick=IN	2	2	6
Thin=IN, Thick=IN	2	2	7
Thin=OUT, Thick=OUT	3 (20-30%)	3 (25%)	6
Thin=IN, Thick=OUT	3	3	7
Thin=OUT, Thick=IN	3	3	8
Thin=IN, Thick=IN	3	3	9
Thin=OUT, Thick=OUT	4 (10-20%)	5 (18%)	8
Thin=IN, Thick=OUT	4	5	9
Thin=OUT, Thick=IN	4	5	10
Thin=IN, Thick=IN	4	5	11
Thin=OUT, Thick=OUT	5 (5-10%)	7 (12%)	10
Thin=IN, Thick=OUT	5	7	11
Thin=OUT, Thick=IN	5	7	12
Thin=IN, Thick=IN	5	7	13
Thin=OUT, Thick=OUT	6 (2-5%)	11 (8%)	12
Thin=IN, Thick=OUT	6	8	13
Thin=OUT, Thick=IN	6	8	14
Thin=IN, Thick=IN	6	8	15
Thin=OUT, Thick=OUT	7 (1-2%)	15 (6%)	15
Thin=IN, Thick=OUT	7	15	15
Thin=OUT, Thick=IN	7	15	15
Thin=IN, Thick=IN	7	15	15

5. Decimation Control Telemetry

Both the State Of Health (SOH) and the packet header telemetry should include the state of the front decimators. Given the space limitations, the full state of the controls shall not be included. Instead a code from which the state can be inferred shall be used. This implies some coordination between the commanding of the front segment control table and the ground software. An 8-bit code shall be used to indicate what Detector Interface Control Table (DICT) is in effect. The DICT includes the front segment decimation state table above, plus the detector interface controls for the rear segment decimation, thresholds, test pulsers, and enables. DICTs shall be assigned an ID number when they are generated. Ground data analysis software shall need to know the contents of each DICT so the state of the decimators and other controls can be inferred. In addition to the DICT ID, the actuator state and the SSR state must be known. So both the packet header and the SOH shall include the DICT ID, the attenuator state, and the SSR state.